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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX INCORPORATED, et al., Defendants.	**CASE NO. C-03-4669-MJJ (EMC)** **CASE NO. C-03-2289-MJJ (EMC)**
SYNOPSYS, INC., Plaintiff, vs. RICOH COMPANY, LTD., Defendant.	**DECLARATION OF DEANNA ALLEN IN SUPPORT OF RICOH'S OPPOSITION TO SYNOPSYS AND DEFENDANTS' MOTION REQUESTING EQUAL PRESENTATION TIME AT TUTORIAL** **Date: To Be Determined** **Time: To Be Determined** **Courtroom: 11** **Judge: Martin J. Jenkins**

DeAnna Allen declares as follows:

1. My name is DeAnna Allen. I am an attorney with the law firm of Dickstein Shapiro Morin & Oshinsky LLP, counsel for Ricoh Company, Ltd. I am over the age of 21 and am competent to make this Declaration. Based on my personal knowledge and information, I hereby declare to all the facts in this Declaration.

2. Attached hereto as Exhibit 1 is a true and correct copy of a September 20, 2004 transmittal letter from DeAnna Allen to Matthew Hocker.

3. Attached hereto as Exhibit 2 is a true and correct copy of the September 20, 2004 draft tutorial outline of Dr. Donald Soderman that was transmitted as an attachment to Exhibit 1 hereof.

4. Attached hereto as Exhibit 3 is a true and correct copy of the September 20, 2004 draft tutorial outline of Synopsys and Defendants.

5. Attached hereto as Exhibit 4 is a true and correct copy of an October 1, 2004 letter from Gary Hoffman to Tom Mavrakakis.

6. Attached hereto as Exhibit 5 is a true and correct copy of an October 1, 2004 letter from Tom Mavrakakis to Gary Hoffman.

7. Attached hereto as Exhibit 6 is a true and correct copy of the parties' July 15, 2004 Joint Claim Construction & Prehearing Statement, including Ex. A thereto.

8. Attached hereto as Exhibit 7 is a true and correct copy of Synopsys and Defendants' September 14, 2004 Responsive Claim Construction Brief for U.S. Patent 4,922, 432 (Re-Filed).

9. Attached hereto as Exhibit 8 is a true and correct copy of U.S. Patent 4,922, 432.

10. Attached hereto as Exhibit 9 is a true and correct copy of an October 13, 2004 transmittal letter from DeAnna Allen to Tom Mavrakakis and an attached draft tutorial outline of Dr. Donald Soderman.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. Signed at Washington, DC on October 13, 2004.

October 13, 2004

/s/ DeAnn Allen
DeAnna Allen

EXHIBIT 1

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September 20, 2004

VIA FACSIMILE AND U.S. MAIL
Matthew E. Hocker, Esq.
Howrey Simon Arnold & White, LLP
301 Ravenswood Avenue
Menlo Park, CA 94025

Re: *Synopsys Inc.* v. *Ricoh Company, Ltd*
Ricoh Company, Ltd. v. Aeroflex Incorporated, et al.
Our Ref.: R2180.0171

Dear Matthew:

As we agreed, attached is Ricoh's outline of the tutorial presentation for the Markman proceedings.

Sincerely,

DeAnna Allen

Enclosure

cc: Thomas C. Mavrakakis, Esq. (w/enclosure)
Christopher Kelley, Esq. (w/enclosure)

EXHIBIT 2

September 20, 2004
6:55 pm EDT

I. Introduction

A. Dr. Donald A. Soderman

B. **[VISUAL]** Background

1. Education

2. Work Experience

3. Experience in ASIC Industry

II. ASICs

A. **[VISUAL]** ASIC- as described in the '432 patent is a specialized integrated circuit chip "designed to perform a specific function."[1]

B. **[VISUAL]** Non-ASIC- "standard, general purpose integrated circuit chips, such as microprocessors, memory chips, etc."[2]

C. **[VISUAL]** Many products common in today's market use ASICs.

D. **[VISUAL]** ASICs have many advantages over general purpose ICs including, that ASICs are smaller, have lower cost and have higher performance.

III. Evolution of ASIC

A. Around 1980, ASICs were simple circuits that very few people were using and even fewer were designing.

B. **[VISUAL]** "In the design process, the VLSI design engineer will consider the particular objectives to be accomplished and tasks to be performed by the integrated circuit and will create structural level design specifications which define the various hardware components required to perform the desired function, as well as the interconnection requirements between these components."[3]

C. **[VISUAL]** Structural level hardware descriptions are descriptions of the architecture or structure (e.g., logic gates, flip flops, etc.) of the circuit desired to be produced as an ASIC, and an example of such a description can be seen from Fig. 1b of the '432 patent.[4] Frequently this done by implicit or explicit selection of gates.

D. **[VISUAL]** In the late 1980's advances in very large scale integrated (VLSI) circuits allowed more highly complex circuits to be integrated on a single chip. This led to the use of ASICs in rapidly expanding list of specific applications, at a faster

design rate, in larger quantities.[5] This led to the need to resolve the following PROBLEMS:

1. **[VISUAL]** "There is only a small number of VLSI designers who possess the highly specialized skills needed to create structural level integrated circuit hardware descriptions."[6]

2. **[VISUAL]** Even with then existing CAD tools that facilitate parts of the process (i.e., layout design), "the design process is time consuming."[7] For example, using such CAD tools, the manufacture of an ASIC for a video camera could require 9 months to a year for design, and an additional 3 or more months for production. At times, the design portion of the process could take longer than a year and sometimes nearly the life cycle of the ASIC. (The life cycle of any particular ASIC was often only a few years.)

3. **[VISUAL]** "[T]he probability of error is also high because of human involvements"[8] and the cost even greater. Designer's working at the structural level commonly made errors in their design specifications, such as choosing the wrong hardware components for a schematic or drawing the wrong wire connections between hardware components in a schematic. An error in the original design, for example, could require months of redesign effort. Errors often were not detected until product testing, after which the manufacturing team needed to find the error, make the design change, release new mask sets, and produce new wafers.

IV. Overview of Manufacturing

A. **[VISUAL]** The manufacturing process is made up of two parts: design and production.

B. **[VISUAL]** In prior art ASIC design, designers commonly created structural descriptions of the circuit desired to be produced. The individual circuit components described in the structural descriptions (Fig. 1b), however, are not individually assembled and placed on the ASIC. Instead, the component circuitry is built-up in layers of complex patterns of semiconductor material (e.g., silicon dioxide, polysilicon, metal, etc.).

C. **[VISUAL]** From the structural description, ASIC designers would create a physical description (known as a "layout") needed to directly produce the ASIC.[9] An exemplary layout representation is shown in Fig. 1c of the '432 patent. The layout representation provides the physical ("geometrical") data needed to produce the ASIC. In particular, the layout is made up of a series of "mask" layers or levels. Each "mask" stencils a pattern for a given layer of the ASIC. When taken together,

the different circuit patterns (or mask levels) make up the circuitry of the desired ASIC. (The data describing the layout representation is known as "mask data" because it describes the different mask levels used in producing the ASIC.)

D. Production of the ASIC:

1. **[VISUAL]** In the production of ASICs, as with other integrated circuit chips, a piece of semiconductor material is provided as a base or initial layer (known as a "substrate") on which other semiconductor material is then deposited. Typically, the base semiconductor material is silicon. The piece of semiconductor material, silicon for example purposes, is typically in the form of a thinly sliced "wafer".

2. **[VISUAL]** A netlist comprising data describing structural ASIC components is directly used to create the layout for the mask data from which mask level patterns are created. As part of ASIC production, each of the mask level patterns generated from the netlist is transferred to the wafer. Each mask level pattern corresponds to one layer for the components that comprise the ASIC. To produce the ASIC as designed, the silicon wafer is covered with a first layer of material that does not conduct electricity (for example "silicon dioxide"). In order to build a first layer for the ASIC components, light-sensitive material (known as "photoresist") is placed over the silicon dioxide. A first mask level is placed over the wafer and light (typically ultraviolet light) is transmitted through the pattern in the mask level to the photoresist on the wafer. The photoresist is chemically responsive to the light so that selected areas corresponding to the mask level pattern are formed in the photoresist.

3. **[VISUAL]** A process known as "etching" is applied to the photoresist. Etching transfers the mask level pattern in the photoresist so that a corresponding pattern of selected areas are formed in the layer of silicon dioxide below. Based on the pattern formed in the oxide, a layer of semiconductor material for the ASIC components is produced on the ASIC.

4. **[VISUAL]** In order to produce a next layer for the ASIC components, the previous, patterned layer of oxide is removed and replaced with a new, unpatterned oxide layer. A layer of polysilicon and a new layer of photoresist are applied. Using a second mask level pattern, the process repeats the steps of transferring the mask level pattern to the photoresist layer and then to the oxide layer to create corresponding selected areas. A second layer of semiconductor material for the ASIC components corresponding to the second mask level is

then produced based on the oxide layer pattern. Each subsequent layer of semiconductor material for the ASIC components is produced in a similar manner using the successive mask levels generated from the mask data and netlist.

V. Process Patented in '432 Patent

A. Advantages:

1. **[VISUAL]** The patented process simplifies the process of designing and producing ASICs, and makes the process quicker, less expensive, and more reliable. Using the invention, a designer is able to define the ASIC using architectural independent functional descriptions (e.g., functional HDLs (Behavioral level descriptions or Functional RTL), and functional graphical representations) as contrasted to structural (architecturally dependent) components (e.g., structural schematics, structural flowcharts, structural netlists, structural RTL, and Boolean Equations). The invention uses the architecture independent functional representations and "generates therefrom the detailed information needed for directly producing an application specific integrated circuit (ASIC) to carry out those specific functions."[10]

2. **[VISUAL]** The patented process, "for the first time, opens the possibility for the design and production of ASICs by designers, engineers and technicians who may not possess the specialized expert knowledge of a highly skilled VLSI design engineer."[11]

B. Process:

1. Describing Actions and Conditions-

a. **[VISUAL]** A designer prepares a description (known as a "specification") of the function or behavior of the ASIC (or portion) that is to be produced. The input description "can be defined in a suitable manner" or format.[12]

b. **[VISUAL]** A graphical example of the functional input description is a flowchart. The patent also states that the same specification can be provided in a textual format, such as in a list form that provides a listing of statements describing the desired functions to be performed by the ASIC.

c. **[VISUAL]** In accordance with the patented process, the designer need not be familiar with the hardware components or other structure that

is to be included in the ASIC. Thus, the input description or specification does not have to specify the structure or architectural components that are to be included in the ASIC to be produced. The input specification is thus referred to as "architecture independent."

d. **[VISUAL]** The description of architecture independent functions are made up of the operations or "actions" to be performed by (or within) the ASIC and the "conditions" under which such actions are to be performed. The architecture independent specifications do not specify or imply the specific structure to be designed.

2. Storing in a Knowledge Base-

a. **[VISUAL]** The patented process uses a storehouse or database of knowledge (known as a "knowledge base") to serve as a base for reference in designing an ASIC. In particular, in accordance with the '432 patent, the knowledge held by experts in VLSI design is obtained and stored in the knowledge base.[13] The expert knowledge is stored in the knowledge base using "rules."[14]

b. **[VISUAL]** "Rules" are prescribed guides or accepted procedures. In the context of the '432 patent, the rules are used to apply the expert knowledge captured from VLSI designers to automatically design an ASIC. The "rules" can take any of a variety of formats. In the preferred embodiment, for example, the rules can be represented using an "IF-THEN" format.[15] Other formats are possible, such as pattern-match or other antecedent-consequent format.

3. Storing a Set of Definitions-

a. **[VISUAL]** The functional input specification is translated or "mapped" to an intermediate form to facilitate use by any system used to perform the process. In particular, the desired functions (in the form of "architecture independent actions and conditions") are associated with (or "mapped") to a set of definitions of the architecture independent actions and conditions.[16]

b. **[VISUAL]** In the '432 patent specification, an exemplary embodiment uses definitions in the

form of code words ("referred to as "macros") representative of a desired function.[17]

c. **[VISUAL]** The set of definitions are typically stored in a library. In the exemplary embodiment disclosed in the '432 patent, the definitions are stored as "macros" in a "macro library."[18] Examples of "macros" can be seen from Table 1 of the '432 patent.[19]

4. Storing Hardware Cells-

a. **[VISUAL]** The hardware components to be used in the design of the ASIC to be produced are referred to as "hardware cells." The hardware cells are basic circuit components (e.g., logic gates, transistors, etc.) that have been previously designed by VLSI engineers, having various functional and technical specifications.[20] A set of available hardware cells that can be used in the design of the ASIC is stored in a "hardware cell library."[21]

5. Operation of the Patented Process

a. **[VISUAL]** The process starts with a user describing a series of architecture independent functional actions and conditions to be performed by the ASIC to be produced.

b. **[VISUAL]** Definitions are then specified from the library of definitions for the desired actions and conditions as described by the user.

c. **[VISUAL]** Hardware cells capable of performing the desired actions and conditions are selected from the hardware cell library by applying the expert knowledge encoded in the rules stored in the expert system knowledge base.

d. **[VISUAL]** A listing of the hardware cells as selected are listed, together with a listing of the connections between such cells, in what is known as a "netlist."

e. **[VISUAL]** The netlist is transformed into a layout of hardware cells that is used to produce the mask data that is directly used for the production of the desired ASIC.

f. **[VISUAL]** The process also involves the generation of signal lines carrying data signals (known as "data paths").[22] This generation of "data paths" can be performed, like the selection

of hardware cells, through the application of expert rules stored in a knowledge base to the selected cells.[23]

g. **[VISUAL]** The process further involves the generation of control signals (known as "control paths") between the hardware cells.[24]

h. **[VISUAL]** Performing the inventive process effectively replaces the need for an expert circuit designer who was, before the invention, required to apply the designer's expertise to the design process to create structural and layout representations of the design.

i. **[VISUAL]** Without the burden of designing the specific structure and layout, even the design engineers who do not have the specialized knowledge of VLSI design could successfully design ASICs faster and more accurately.

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[1] '432 Patent at 1:13-17.
[2] '432 Patent at 1:13-17.
[3] '432 Patent at 1:19-26.
[4] '432 Patent at 1:19-26; and 3:59-65.
[5] '432 Patent at 1:45-51.
[6] '432 Patent at 1:63-66.
[7] '432 Patent at 1:66 to 2:1.
[8] '432 Patent at 1:66 to 2:1.
[9] '432 Patent at 1:38-44.
[10] '432 Patent at 2:6-14.
[11] '432 Patent at 2:14-20.
[12] '432 Patent at 2:21-24.
[13] '432 Patent at 5:6-8.
[14] '432 Patent at 8:65 to 9:5.
[15] '432 Patent at 11:1-14.
[16] '432 Patent at 9:8-18; and 13:2-31.
[17] '432 Patent at 5:20-22.
[18] '432 Patent at 5:20-22.
[19] '432 Patent at 5:20-22.
[20] '432 Patent at 5:15-20.
[21] '432 Patent at 4:68 to 5:3.
[22] '432 Patent at 2:39-40; and 6:28-54.
[23] '432 Patent at 4:63 to 5:13; and 13:55-56.
[24] '432 Patent at 2:36-44; and 4:63 to 5:13.

EXHIBIT 3

HOWREY SIMON ARNOLD & WHITE HOWREY LLP ATTORNEYS AT LAW

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September 20, 2004

VIA FACSIMILE AND FEDERAL EXPRESS

Kenneth W. Brothers, Esq.
Dickstein Shapiro Morin & Oshinsky LLP
2101 L Street NW
Washington, DC 20037-15226

RE: Synopsys, Inc. v. Ricoh Company, Ltd.
Ricoh Company, Ltd. v. Aeroflex, Incorporated, et al.

Dear Mr. Brothers:

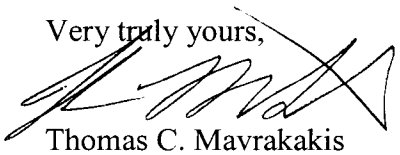
I am writing to follow-up on the issues between the parties regarding the claim construction tutorial scheduled for October 20, 2004.

Synopsys and Defendants do not believe that any alleged expert hired by Ricoh and directed by your firm will present a neutral view of the '432 patent or any related background information at the tutorial. If Ricoh continues to insist that its expert make any presentation at the tutorial, Synopsys and Defendants will make their own presentation using their own expert.

It is our understanding that the latest proposal is that the parties exchange, by facsimile, preliminary proposed outlines for their respective presentations today. Synopsys and Defendants provide the attached outline of preliminary proposed points for facilitating the parties' meet and confer regarding the substance of the tutorial.

Finally, Synopsys and Defendants believe that the EDA Consortium's video "EDA – Where Electronics Begins" would be helpful to the Court and therefore, plan on showing that video to the Court at the tutorial. The web address http://www.edac.org/ is where that video can be viewed online.

Very truly yours,



Thomas C. Mavrakakis

tcm:sjc

cc: Edward M. Meilman, Esq.

Synopsys' and Defendants' Preliminary Proposed Points For The Tutorial

- '432 patent's invention is directed to a computer-aided design system and method for designing application specific integrated circuits, which are commonly known by the acronym ASIC;
- An integrated circuit is comprised of the necessary devices and their interconnections necessary to create a complete circuit all on one silicon substrate;
- There are two types of integrated circuits "application specific" and "general purpose";
- The '432 patent is directed to using computers to design ASICs as opposed to standard general purpose integrated circuits;
- The '432 patent is not directed to designing microprocessors, memory chips, or other general purpose chips;
- A remote car alarm and keyless entry transmitter for cars would be an example of things that use an ASIC;
- The processors in a cell phone would be examples of general purpose integrated circuits;
- FIG. 2 shows the knowledge-based silicon compiler is used to generate a netlist from a flowchart;
- FIG. 2 also shows that other computer-aided design software tools not described in the '432 patent are used to generate mask data from a netlist;
- FIG. 5 shows the input flowchart created using the flowchart editor program by representing the sequence of actions (rectangles) and decisions (diamonds) and then specifying a macro (e.g., add or compare) for each of those actions and conditions;
- The flowchart editor program achieves the '432 patent's goal of eliminating the need for using highly skilled VLSI designers to design ASICs;
- Writing HDL requires highly skilled VLSI designers to design ASICs;
- Hardware description languages have been used by highly skilled VLSI designers for describing hardware designs since the mid-1970s;
- Conventional software programs use predefined step-by-step procedures (or algorithms) to solve problems;
- Expert system software such as described in the '432 patent are substantially different from conventional software and use a knowledge base containing rules in a particular field, and a separate inference engine software program for selectively applying the rules in the knowledge base to solve the problem;
- FIG. 15 shows a netlist having hardware cells, a system controller, and control and data paths for interconnecting them;
- One example computer-aided design tool needed for generating mask data is known as "placing," which enables a designer to plan the location of the circuit blocks in the design;
- FIG. 1c pictorially illustrates mask data;
- The software programs for implementing the '432 patent's methods are illustrated in FIG. 3;

- TABLE 1 in the '432 patent shows the stored actions and conditions that are available and may be specified in the flowchart;
- The '432 patent sets forth the four types of information that are stored for each hardware cell and that is necessary for mapping corresponding hardware cells to the macros specified in the flowchart, generating the netlist, and generating mask data;
- The '432 patent uses a rule-based expert system for mapping corresponding hardware cells to the macros specified in the flowchart;
- The '432 patent uses IF-THEN rules having both an antecedent (IF) and a consequent (THEN) portions;
- The inference strategy for the inference engine is described in the '432 patent;
- Describing the sequence of operations is the first step performed by the designer using the flowchart editor to define the flowchart input;
- The rectangles represent the actions, the diamonds represent the conditions, and the lines with arrows represent the transitions between them and together the rectangles, diamonds, and lines with arrows represent the series of actions and conditions for the ASIC to be designed;
- Specifying one macro in the macro library for each rectangle and diamond is the second step performed by the designer using the flowchart editor to define the flowchart input;
- For each specified macro in the flowchart, the rule-based expert system's inference engine selectively applies rules in the knowledge base to map each macro to a corresponding hardware cell description and this is illustrated in FIG.4 and FIG. 11;
- The example rules in the '432 patent show that a system controller hardware cell must be generated for the netlist and this is illustrated in FIG. 12;
- The example rules in the '432 patent show that control and data paths must be generated for the netlist and this is illustrated in FIG. 13;
- The example rules in the '432 patent show that eliminating unnecessary selected hardware cells must be done for generating a netlist and this is illustrated in FIG. 15;
- The '432 patent only has 10 example rules and it would take at least 500 or more rules to have an operational system;
- The '432 patent does not describe software for generating mask data but merely suggests using other unidentified computer-aided software design tools;
- Mask data represents the various layers that form the devices and interconnections of the ASIC design;
- The mask data is the information that is eventually used by photomask manufacturers to make the set of 20 or more photomasks (or masks) that are used in the manufacturing processes for the ASIC;
- The '432 patent does not describe any processes for manufacturing photomasks or ASICs;
- The manufacturing processes such as chemical vapor deposition, physical vapor deposition, ion implant, chemical mechanical polishing, etc. form the devices and interconnections of the ASIC.

EXHIBIT 4

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October 1, 2004

BY FACSIMILE and US Mail

Tom Mavrakakis, Esq.
Howrey Simon Arnold & White LLP
301 Ravenswood Ave.
Menlo Park, CA 94025

Re: Ricoh v. Aeroflex et al.

Dear Tom:

I have your letter of September 28, 2004. It is in part incomplete and in part inaccurate. I will therefore reiterate some of the points discussed and agreements reached.

First, as discussed in our meet and confer of September 28, 2004, we agreed on a process for trying to locate a potential independent expert for the upcoming Markman tutorial before Judge Jenkins. I told you, and it bears repeating here, that Ricoh does not agree that Judge Jenkins has required an independent, mutually-selected expert for the tutorial or that such a mutually-selected expert is needed. Judge Jenkins explicitly stated that the tutorial is a "very plaintiff presentation." Nevertheless, we will consider identified experts who at a minimum meet the criteria stated in my letter of September 27, 2004. Also, any person who does or has done business with, or whose work is or has been sponsored by any of the parties or their licensees would not be a neutral independent expert. In the event that Synopsys/ASIC Defendants or Ricoh (each individually a "party" and collectively "the parties") proposes an independent expert as a potential neutral expert for the tutorial, the parties have agreed to the following:

- No party shall approach or otherwise engage in any contact or discussions with the identified expert except as mutually agreed to in advance and in writing by the parties.

- Once identified, neither party shall engage or otherwise have discussions with the expert in connection with the present litigation matters for any reason or purpose other than to serve as a mutually selected, independent neutral expert at the Markman tutorial. However, nothing stated herein shall effect or otherwise limit a party's right to engage or have discussions with a proposed expert where, prior to the expert's identification as a potential independent expert at the tutorial, the party had contacted the expert in connection with the present litigation matters. If a party wants to

have such future discussions with such expert then evidence of such prior contact shall, on request, be provided to the other party.

- No party shall waive any right to make reasonable objections on the basis of the proposed expert's qualifications, neutrality, or on any other basis, regardless of whether the objecting party (or another party) identified the expert as a potential independent neutral expert.

- No party shall rely in any manner on the use or procurement of (or on the failure to use or procure) an independent neutral expert in order to delay, alter or otherwise modify the scheduled Markman tutorial and hearing dates of October 20, and 29, respectively.

You have identified Rev. McFarland and Professor Rabaey as potential neutral experts. Neither meet the agreed upon criteria for an independent neutral expert. Regarding Rev. McFarland, not only did you list him in your initial disclosures, but we previously contacted him in connection with this litigation . Regarding Professor Rabaey, he is a professor at the University of California at Berkeley and receives support from Synopsys as part of the Synopsys University Program. In fact, Synopsys has previously quoted Professor Rabaey's statement acknowledging the importance of Synopsys' support in advancing the research and education programs in his department (i.e., at the Berkeley Wireless Research Center). Consequently, neither of these people satisfy the agreed upon criteria.

At the September 28 meet and confer, we disagreed with your proposal that Synopsys and the ASIC Defendants have unfettered veto power over everything Ricoh may wish to present at the tutorial. On the other hand, I did ask you to identify any matter in our detailed proposal that you considered improper or inaccurate and offered to do the same with your bullet point outline proposal. In particular, I extended an offer to simultaneously exchange markups of the September 20, 2004 tutorial outline drafts. During our conference call on Tuesday, September 28, you had indicated that you would get back to us within 30 minutes on this proposal; it is now three (3) days later and we still have not heard back from you on the proposal.

We are disappointed that you have refused to cooperate in the formulation of the tutorial presentation. Nevertheless, our offer still remains open.

Very truly yours,

Gary M. Hoffman

GMH/dda
cc: Janna Whitte
Edward Meilman, Esq.

FAX TRANSMISSION

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP

DATE: October 1, 2004

CLIENT NO.: R2180.0171

MESSAGE TO: Thomas C. Mavrakakis

cc: Janna White

COMPANY: Howrey Simon Arnold & White LLP

FAX NUMBER: (650) 463-8400

PHONE: (650) 463-8100

FROM: Gary M. Hoffman

PHONE: (202) 572-2656

PAGES (Including Cover Sheet): 3 **HARD COPY TO FOLLOW:** X **YES** ____ **NO**

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MESSAGE:

If your receipt of this transmission is in error, please notify this firm immediately by collect call to our Facsimile Department at 202-861-9106, and send the original transmission to us by return mail at the address below.

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FAX TRANSMISSION

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP

DATE: October 1, 2004

CLIENT NO.: R2180.0171

MESSAGE TO: Thomas C. Mavrakakis

cc: Janna White

COMPANY: Howrey Simon Arnold & White LLP

FAX NUMBER: (650) 463-8400

PHONE: (650) 463-8100

FROM: Gary M. Hoffman

PHONE: (202) 572-2656

PAGES (Including Cover Sheet): 3 **HARD COPY TO FOLLOW:** X YES ____ NO

SENT BY:		DATE/TIME:	

MESSAGE:

EXHIBIT 5

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October 1, 2004

BY FACSIMILE AND U.S. MAIL

Gary M. Hoffman, Esq.
Dickstein Shapiro Morin & Oshinsky LLP
2101 L Street NW
Washington, DC 20037

RE: Synopsys, Inc v. Ricoh Company, Ltd.
Case No. CV 03-02289 MJJ (EMC)
Ricoh Company, Ltd. v. Aeroflex, Inc.
Case No. CV 03-04669 MJJ (EMC)

Dear Mr. Hoffman:

I am writing in response to your letter and voicemail today regarding the tutorial. You seem to have misunderstood my letter of September 28, 2004.

Ricoh's position that it will unilaterally determine the final content of the tutorial presentation including the script of what is said by the expert at the tutorial is not reasonable and not acceptable to Synopsys and Defendants. Synopsys and Defendants believe that their agreement to the final content of the tutorial presentation including the script of what is said by the expert is essential for a neutral tutorial. We do not understand how you could legitimately believe that there is any need for any further meet and confer given this basic disagreement between the parties.

We will seek an order from the Court that precludes Ricoh from presenting expert testimony on claim construction at the tutorial and that allows Synopsys and Defendants equal time on October 20, 2004 to make their own presentation at the tutorial. Please let me know on Monday, October 4, 2004 whether Ricoh will agree to a shortened briefing schedule so that the Court may resolve this issue before the end of next week.

Very truly yours,

Thomas C. Mavrakakis

tcm:sjc
cc: Edward Meilman, Esq.

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DATE: October 1, 2004

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☒ **ORIGINAL WILL FOLLOW VIA:**
☒ REGULAR MAIL ☐ OVERNIGHT DELIVERY ☐ HAND DELIVERY ☐ OTHER:

☐ **ORIGINAL WILL NOT FOLLOW**

SUPPLEMENTAL MESSAGE:

Please see attached letter of this date from Thomas C. Mavrakakis.

EXHIBIT 6

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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX INCORPORATED, et al., Defendants	**CASE NO. C-03-4669-MJJ (EMC)** **CASE NO. C-03-2289-MJJ (EMC)**
SYNOPSYS, INC., Plaintiff, vs. RICOH COMPANY, LTD., Defendant	**JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT** **Date: October 20, 2004** **Time: 2:30 p.m.** **Courtroom: 11**

Pursuant to Patent L.R. 4-3, plaintiff and declaratory judgment defendant Ricoh Company, Ltd. ("Ricoh"), declaratory judgment plaintiff Synopsys, Inc., ("Synopsys"), and defendants and declaratory judgment counterclaimants Aeroflex, et al. ("Aeroflex") (collectively, "the Parties") submit their joint claim construction in the chart attached as Exhibit A.

Statement regarding subsection (a): The parties have been unable to agree on any proposed construction of the claim language for claims 13-17 of the '432 patent.

Statement regarding subsection (b): Exhibit A contains each Party's proposed construction of each disputed claim term, phrase or clause, together with an identification of all references from the '432 patent's specification and/or the '432 patent's prosecution (or file) history that support that construction. It also identifies all extrinsic evidence known to the party on which it intends to rely either to support its proposed construction of each disputed claim term, phrase or clause or to oppose any other party's proposed construction of each disputed claim term, phrase or clause, including but not limited to, as permitted by law, dictionary definitions, citations to learned treatises and prior art, and testimony of percipient and expert witnesses. Synopsys and the Defendants have attached the identified intrinsic and extrinsic evidence as well as dictionaries, etc. to Exhibit A.

Statement regarding subsection (c): The Parties agree that the amount of time for the tutorial (scheduled for October 20, 2004, at 2:30 p.m.) and the claim construction hearing (scheduled for October 29, 2004, at 9:30 a.m.) should be evenly divided between Ricoh, on the one hand, and Synopsys and the Aeroflex et al. defendants, on the other hand.

Statement regarding subsection (d): No Party proposes to call percipient witnesses at either the tutorial or the claim construction hearing. Pursuant to the Court's directives at the telephone hearing on July 14, 2004, Ricoh has not cited extrinsic evidence. Ricoh objects to the citation of extrinsic evidence by Synopsys and Aeroflex, and reserves its right to seek discovery regarding any such extrinsic evidence and respond with its own extrinsic evidence. Attached as Exhibit B is a summary of the testimony of Thaddeus J. Kowalski, Ph.D., an expert witness on behalf of Synopsys and the Aeroflex et al. defendants, supporting Synopsys' and the Aeroflex et

al. defendants' proposed constructions and opposing Ricoh's proposed constructions for each disputed claim term, phrase or clause.

Statement regarding subsection (e): The prehearing conference and tutorial is scheduled for October 20, 2004 at 2:30 p.m. Other than the dispute referenced in the parties' July 15, 2004, joint letter to the Court, the parties are not aware of any other issues at this time.

Dated: July 15, 2004

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Exhibit A ('432 Patent)

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
13. A computer-aided design process for designing an application specific integrated circuit which will perform a desired function comprising	During manufacture of a desired application specific integrated circuit (ASIC) chip that is designed to perform a specific purpose, a process of designing the desired ASIC using a computer, the process comprising: ("application specific integrated circuit (ASIC)"= an integrated circuit chip designed to perform a specific function.) <u>Support</u> '432 Patent: Column 1, lines 13-17; column 2, lines 15-20. RCL000207-223. "computer-aided design": The use of computers to aid in design layout and analysis. IEEE Standard Dictionary of Electrical and Electronic Terms,	A. "A computer-aided design process for designing" -- a process that uses a computer for designing, as distinguished from a computer-aided manufacturing process, which uses a computer to direct and control the manufacturing process. *Intrinsic Evidence:* **'432 patent:** 1:9-12; 16:34-65 [Attachment 2[1], DEF012564-DEF012585]. *Extrinsic Evidence:* **Decl. Kowalski** ¶¶ 16-18[2]; **CAD Tool Integration For ASIC Design:** at 364-365 [Attachment 21, KBSC000031-KBSC000036]. *Dictionaries, Treatises, Textbooks, etc.:* **IBM Dictionary of Computing:** at 129-130 [Attachment 16, DEF083932-DEF084703]; **IC Mask Design:** at 1-24 Attachment 17,

[1] Referenced attachments are attached to this Exhibit A.

[2] "Decl. Kowalski ¶ ¶" refers to the pertinent paragraphs in the Declaration and Summary of Opinions of Dr. Thaddeus J. Kowalski on Construction of Disputed Claim Terms of United States Patent No. 4,922,432 that support Synopsys' and Defendants' proposed constructions and oppose Ricoh's proposed constructions for the disputed claim term, phrase or clause. Ricoh objects to the citation of extrinsic evidence by Synopsys and the Aeroflex defendants, and reserves its right to seek discovery regarding any such extrinsic evidence and respond with its own extrinsic evidence.

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
	Fourth Edition (1988). RCL011382-388 at RCL011384. "function": A specific purpose of an entity or its characteristic action. IEEE Standard Dictionary of Electrical and Electronic Terms, Fourth Edition (1988). RCL011382-388 at RCL011386. "function": Any of a group of related actions contributing to a larger action. Merriam-Merriam-Webster's Ninth New Collegiate Dictionary (1987). RCL011389-407 at RCL011400.	DEF085303-DEF085329]; **Microchip Fabrication:** at 76-82, 274-278 [Attachment 18, DEF085330-085343]; **IEEE Standard Dictionary of Electrical and Electronics Terms:** at 180 [Attachment 19, DEF085299-085302]; **Webster's Dictionary:** at 343, 725 [Attachment 20, DEF085290-DEF085298]. B. "application specific integrated circuit" -- an interconnected miniaturized electronic circuit on a single piece of semiconductor material designed to perform a specific function, as distinguished from standard, general purpose integrated circuits, such as microprocessors, memory chips, etc. *Intrinsic Evidence:* **'432 patent:** 1:13-17; 16:34-65 [Attachment 2, DEF012564-DEF012585]. *Extrinsic Evidence:* **Decl. Kowalski** ¶¶ 19-20; **CAD Tool Integration For ASIC Design:** at 363 [Attachment 21, KBSC000031-KBSC000036].

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
storing a set of definitions of architecture independent actions and conditions;	Placing in computer memory a library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC, where the architecture independent actions and conditions do not imply any structure or implementing technology. ("architecture independent action and condition"= functional or behavioral aspects of a portion of a circuit (or circuit segment) that does not imply any set architecture, structure or implementing technology.) <u>Support</u> '432 Patent: Figs. 1a, 1b, 1c, 4; column 2, lines 6-20; column 2, lines 27-34; column 3, line 49 to column 4, line 4; column 4, lines 5-19; column 5, lines 20-22; column 7, lines 24-50; column 8, lines 23-51; column 10, lines 10-12; column 13, lines 2-31.	C.[3] "actions and conditions"-- are the logical steps and decisions that are represented as rectangles and diamonds in the flowchart; collectively logical operations. *Intrinsic Evidence:* **'432 patent:** 2:24-27; 3:50-59; 4:15-19; 4:61-63; 6:3-14; 7:20-23; 8:47-51; 16:34-65 [Attachment 2, DEF012564-DEF012585]; **'432 patent file history:** April 1989 Amendment at 9, 11; October 1989 Examiner Interview Summary; November 1989 Amendment at 6-7 [Attachment 3, DEF011820-DEF012110]. *Extrinsic Evidence:* **Decl. Kowalski** ¶ 21. *Dictionaries, Treatises, Textbooks, etc.:* **IBM Dictionary of Computing:** at 479 [Attachment 16, DEF083932-DEF084703].

[3] Synopsys and the Defendants disagree with Ricoh's definition of "storing" on this step and the next two steps as "placing in computer memory." Storing means placing on any storage device "that is accessible by the processor for the computer system." IBM Dictionary of Computing at 654 (Attachment 16, DEF083932-DEF084703).

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
	"action": A thing done. Merriam-Webster's Ninth New Collegiate Dictionary (1987). RCL011389-407 at RCL011391. "architecture": A unifying or coherent form or structure. Merriam-Webster's Ninth New Collegiate Dictionary (1987). RCL011389-407 at RCL011393. "independent": Not dependent; not requiring or relying on something else. Merriam-Webster's Ninth New Collegiate Dictionary (1987). RCL011389-407 at RCL011394. "condition": Something essential to the appearance or occurrence of something else. Merriam-Webster's Ninth New Collegiate Dictionary (1987). RCL011389-407 at RCL011405A	D. "architecture independent"[4] -- not including (i.e., excluding) a register transfer level (RTL) description or any other description that is hardware architecture dependent. An RTL description consists of: 1) defining the inputs, outputs, and any registers of the proposed ASIC; and, 2) describing for a single clock cycle of the ASIC how the ASIC outputs and any registers are set according to the values of the ASIC inputs and the previous values of the registers; an RTL description defines any control needed for the ASIC. *Intrinsic Evidence:* **'432 patent file history:** April 1989 Amendment at 8-10, 13; November 1989 Amendment at 7 [Attachment 3, DEF011820-DEF012110]; **'435 patent:** Fig. 4; 4:26-32; 5:27-35 [Attachment 4, DEF012503-DEF012518]. *Extrinsic Evidence:* **Decl. Kowalski** ¶¶ 22-26; **Computer Aided VLSI Design Vol.1 No. 4:** at 388

[4] This phrase was not in the original patent application and therefore violates the prohibition of Section 132 of 35 U.S.C. against adding new matter. Moreover, it is indefinite and inadequately described in the '432 patent. The only description is in the '432 patent's file history, which is in the negative.

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
		[Attachment 22, KBSC001109-KBSC001131]. E. "a set of definitions of architecture independent actions and conditions" -- a set of named descriptions defining the functionality and arguments for the available logical steps and decisions that may be specified in the flowchart; and excluding a register transfer level description. *Intrinsic Evidence:* **'432 patent:** 4:61-63; 5:20-22; 6:3-14; 7:25-50; 8:47-51; 16:34-65 [Attachment 2, DEF012564-DEF012585]. *Extrinsic Evidence:* **Decl. Kowalski** ¶¶ 27-28.
storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set;	Placing in computer memory a library of cell information that describe hardware cells capable of performing the different architecture independent actions and conditions placed in the library of definitions. ("hardware cells"= previously designed circuit components or structure that have specific physical and functional characteristics used as building blocks for implementing an ASIC to be	F. "hardware cells" -- logic blocks for which the functional level (e.g., register transfer level), logic level (e.g., flip flop and gate level), circuit level (e.g., transistor level), and layout level (e.g., geometrical mask level) descriptions are all defined. *Intrinsic Evidence:* **'432 patent:** 2:34-39; 3:59-67; 5:15-20; 9:24-51; 16:34-65; 16:66-68 [Attachment 2, DEF012564-

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
	manufactured.) Support '432 Patent: Fig. 4; column 2, lines 36-39; column 4, line 68 to column 5, line 3; column 5, lines 15-20; column 5, lines 22-25; column 9, lines 24-60; column 10, lines 10-12.	DEF012585]; **'016 patent:** 11:47-13:63; 14:3-22 [Attachment 5, DEF017265-DEF017284]. *Extrinsic Evidence:* **Decl. Kowalski** ¶¶ 29-30; **Computer Aided VLSI Design Vol.1 No. 4:** at 380 [Attachment 22, KBSC001109-KBSC001131]. G. "data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set" -- a set of named integrated circuit hardware cells that includes at least one hardware cell for each stored definition that may be specified for the available logical steps and decisions; where each named hardware cell has corresponding descriptions at the functional level (e.g., register transfer level), logic level (e.g., flip-flop and gate level), circuit level (e.g., transistor level), and layout level (e.g., geometrical mask level) that are all defined. *Intrinsic Evidence:* **'432 patent:** Fig. 4; 2:34-39; 3:59-67; 5:15-20; 5:23-25; 9:24-51; 16:34-65; 16:66-68 [Attachment 2, DEF012564-DEF012585]. *Extrinsic Evidence:*

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
		Decl. Kowalski ¶¶ 31-32.
storing in an expert system knowledge base a set of rules for selecting hardware cells to perform the actions and conditions;	Placing in an expert system knowledge base, that uses a computer memory, a plurality of rules for selecting among the hardware cells placed in the hardware cell library, wherein the rules comprise the expert knowledge of highly skilled VLSI designers formulated as prescribed procedures. ("expert system knowledge base"= database used to store expert knowledge of highly skilled VLSI designers.) ("rules"= the expert knowledge of highly skilled VLSI designers formulated as prescribed procedures.) <u>Support</u> '432 Patent: Column 5, lines 6-8; column 8, line 65 to column 9, line 5; column 9, lines 14-20; column 10, lines 1-10; column 10, line 40 to column 11, line 14; column 11, lines 16-26; column 11, lines 30-32; column 11, line 46 to column 12, line 35. RCL000229-237.	H. "expert system" -- software executing on a computer system that attempts to embody the knowledge of a human expert in a particular field and then uses that knowledge to simulate the reasoning of such an expert to solve problems in that field. This system is comprised of a knowledge base containing rules, working memory containing the problem description, and an inference engine. It solves problems through the selective application of the rules in the knowledge base to the problem description, as distinguished from conventional software, which uses a predefined step-by-step procedure (algorithm) to solve problems. *Intrinsic evidence:* **'432 patent:** 2:58-63; 5:6-8; 8:58-60; 10:39-11:26; 14:50-59; 15:53-58; 16:34-65 [Attachment 2, DEF012564-DEF012585]; **'432 patent's file history:** April 1989 Amendment at 9-11, 15, 17; October 1989 Examiner Interview Summary; November 1989 Amendment at 7, 9 [Attachment 3, DEF011820-012110]; **'016 patent:** 2:65-3:8 [Attachment 5, DEF017265-DEF017284]; **'435 patent**: 7:32-9:35[Attachment 4, DEF012503-

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
	"rule": A prescribed guide for conduct or action; an accepted procedure, custom or habit. Merriam-Webster's Ninth New Collegiate Dictionary (1987). RCL011389-407 at RCL011405. "expert system": (1977): computer software that attempts to mimic the reasoning of a human specialist. Merriam-Webster's Collegiate Dictionary Tenth Edition (1999). RCL011408-410 at RCL011410.	DEF012518]; **'603 patent:** 1:44-49 [Attachment 6, DEF017456-DEF017482]; **An Overview of Logic Synthesis Systems:** at 170 [Attachment 7, DEF011962-DEF011968]; **The CMU Design Automation System:** at 75-77 [Attachment 8, DEF012045-DEF012052]. I. "Knowledge base" -- the portion of the expert system containing a set of rules embodying the expert knowledge for the particular field. *Intrinsic evidence:* **'432 patent:** 10:39-11:15; 14:50-59; 15:53-58; 16:34-65 [Attachment 2, DEF012864-DEF012585]; **'432 patent file history:** April 1989 Amendment at 9-11, 15, 17; October 1989 Examiner Interview Summary; November 1989 Amendment at 7, 9 [Attachment 3, DEF011820-DEF012110]; **'435 patent**: 7:32-9:35 [Attachment 4, DEF012503-DEF012518]. J. "a set of rules for selecting hardware cells to perform the actions and conditions" -- a set of rules, each having an antecedent portion (IF) and a consequent portion (THEN), embodying the knowledge of expert designers for application specific integrated circuits, which enables the

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
		expert system to map the specified stored definitions for each logical step and decision represented in the flowchart to a corresponding stored hardware cell description. *Intrinsic evidence:* **'432 patent:** 2:58-63; 8:20-30; 8:58-9:62; 10:39-11:26; 14:50-59; 15:53-58; 16:34-65 [Attachment 2, DEF012564-DEF012585]; **'432 patent file history:** April 1989 Amendment at 9-11, 15, 17; October 1989 Examiner Interview Summary; November 1989 Amendment at 7, 9 [Attachment 3, DEF011820-DEF012110]; **'435 patent**: 7:32-9:35 [Attachment 4, DEF012503-DEF012518]; **An Overview of Logic Synthesis Systems:** at 170 [Attachment 7, DEF011962-DEF011968]; **The CMU Design Automation System:** at 75-77 [Attachment 8, DEF012045-DEF012052]. *Extrinsic Evidence for all of the above phrases (H, I, & J) in this step:* **Decl. Kowalski** ¶¶ 33-45; **Computer Aided VLSI Design Vol.1 No. 4:** 351, 377-381, 383, 388-389 [Attachment 22, KBSC001109-KBSC001131]; **'669 patent:** Abstract, 1:13-16, 2:28-33, 4:31-62; 5:21-38, 5:58-68, 6:1-7:68, 17:62 [Attachment 23, DEF 080579-DEF080605]; **The VLSI**

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		Design Automation Assistant: at 889-90 [Attachment 28, DEF018660-DEF018664]; **A Rule-Based Logic Circuit Synthesis System for CMOS Gate Arrays**: at 597 [Attachment 29, DEF018277-DEF018283]. *Dictionaries, Treatises, Textbooks, etc. for all of the above phrases (H, I, & J in this step):* **Understanding Expert Systems:** 7-10, 29-30, 40, 42, 74-78, 99-110 [Attachment 24, DEF079512-DEF079741]; **An Artificial Intelligence Approach To VLSI Design:** at 9-15 [Attachment 25, DEF078425-DEF078455]; **Artificial Intelligence Terminology:** at 6 [algorithm], 10 [antecedent], 53 [consequent], 86-87 [expert system], 127 [inference engine], 140 [knowledge based system], 204 [production system], 223 [rule base, rule-based system], 281 [working memory] [Attachment 26, DEF079212-DEF079511]; **Microsoft Press Computer Dictionary:** at 136 [expert system] [Attachment 27, DEF083323-DEF083325]; **IBM Dictionary of Computing:** 591 [rule interpreter, rule-based system] [Attachment 16, DEF083932-DEF084703]; **Expert Systems: A Non-Programmer's Guide:** 8-10, 16 [Attachment 30, DEF082264-DEF082528]; **Expert Systems:**

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
		Tools and Applications: at 269 [Attachment 31, DEF079985-DEF080283]; **Expert Systems: Principles and Case Studies:** at 11-12 [Attachment 32, DEF079753-DEF079984]; **Knowledge-Based Systems: The View in 1986:** at 16 [Attachment 33, DEF083251-DEF083284].
describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions;	A user describing an input specification containing the desired functions to be performed by the desired ASIC. Support '432 Patent: Column 1, line 13 to column 2, line 3, column 2, lines 6-20, column 2, lines 21-24; column 2, lines 27-34; column 6, lines 58-60; column 13, lines 32-35; column 14, lines 7-29. RCL000207-223, RCL000229-237. "describe": To represent or give an account in words <~ a picture>; to represent by a figure, model, or picture: delineate. Merriam-Webster's Ninth New Collegiate Dictionary (1987). RCL011389-407 at RCL011398. "description": A descriptive statement or account.	K. "describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions" -- the designer represents a sequence of logical steps (rectangles) and decisions (diamonds), and the transitions (lines with arrows) between them in a flowchart format for a proposed application specific integrated circuit. *Intrinsic evidence:* **'432 patent:** Figs. 1a, 5, &7; 2:21-27; 3:20-22; 3:50-59; 4:5-22; 4:35-38; 7:12-23; 16:34-65 [Attachment 2, DEF012564-012585]; **'432 patent file history:** April 1989 Amendment at 9, 11; October 1989 Examiner Interview Summary; November 1989 Amendment at 6-7 [Attachment 3, DEF011820-DEF012110]; **'016 patent:** 7:33-9:52 [Attachment 5, DEF017265-DEF017284]; **'435 patent:** 4:26-33 [Attachment 4, DEF012503-DEF012518]; **Flamel: A High-**

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
	Merriam-Webster's Ninth New Collegiate Dictionary (1987). RCL011389-407 at RCL011398.	**Level Hardware Compiler:** 260-261 [Attachment 9, DEF012034-DEF012044]; **An Overview of Logic Synthesis Systems:** at 168-170 [Attachment 7, DEF011962-DEF011968]; **Methods Used in an Automatic Logic Design Generator (ALERT):** at 595 [Attachment 10, DEF011969-DEF011989]; **Quality of Designs From an Automatic Logic Generator (ALERT):** at 71 [Attachment 11, DEF012005-DEF012023]; **The CMU Design Automation System:** at 73-74 [Attachment 8, DEF012045-DEF012052]; **A New Look at Logic Synthesis:** at 544 [Attachment 12, DEF012024-DEF012030]; **Experiments in Logic Synthesis:** at 235 [Attachment 13, DEF011990-DEF011994]; **CAD Systems for IC Design:** at 3, 7 [Attachment 14, DEF011951-DEF011961]; **Verifying Compiled Silicon:** at 2 [Attachment 15, DEF011948-DEF011950]; **'442 patent:** 5:3-46, [Attachment 35, DEF012392-DEF012401; '603 patent: 2:41-61 [Attachment 6, DEF012392-DEF012401]. *Extrinsic Evidence:* **Decl. Kowalski ¶¶** 46-49; **Computer Aided VLSI Design Vol.1 No. 4:** 351, 377-381, 383, 388-389 [Attachment 22, KBSC001109-KBSC001131];

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
		Silicon Compilation: at 48-49 [Attachment 34, DEF076335-DEF076341]. *Dictionaries, Treatises, Textbooks, etc.:* **Webster's Ninth New Collegiate Dictionary** at 343, 1074, 1073 [Attachment 20, DEF085290-DEF085298].
specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed; and	Specifying for each desired function to be performed by the desired ASIC one of the definitions of the architecture independent actions and conditions stored in the library of definitions that is associated with the desired function. ("specifying"= mapping or associating a desired function to be performed by the manufactured ASIC with a definition from the library of definitions.) <u>Support</u> '432 Patent: Column 5, lines 20-22; column 7, lines 24-50; column 8, lines 23-51; column 8, lines 65-67; column 9, lines 8-18; column 10, lines 10-12; column 13, lines 2-31.	L. "specifying for each described action and condition of the series one of said stored definitions" -- the designer assigns one definition from the set of stored definitions for each of the described logical steps and decisions represented in the flowchart. *Intrinsic Evidence:* **'432 patent:** Fig. 5; 3:20-22; 4:61-63; 5:20-22; 7:24-25; 8:23-26; 8:51-56; 16:34-65 [Attachment 2, DEF012564-DEF012585]; **'016 patent:** 6:12-32 [Attachment 5, DEF017265-DEF017284]. *Dictionaries, Treatises, Textbooks, etc.* **Webster's Ninth New Collegiate Dictionary** at 1132 [Attachment 20, DEF085290-DEF085298]. M. "which corresponds to the desired action or condition to be performed" -- each specified definition must correspond to the intended step or

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
		decision to be performed. *Intrinsic Evidence:* **'432 patent:** Fig. 5; 3:20-22; 4:61-63; 5:20-22; 7:24-25; 8:23-26; 8:51-56; 16:34-65 [Attachment 2, DEF012564-DEF012585]; **'016 patent:** 6:12-32 [Attachment 5, DEF017265-DEF017284]. *Extrinsic Evidence:* **Decl. Kowalski** ¶¶ 50-52. *Dictionaries, Treatises, Textbooks, etc.:* **Webster's Ninth New Collegiate Dictionary** at 110 [Attachment 20, DEF085290-DEF085298].
selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit, said step of selecting a hardware	Selecting from the plurality of hardware cells in the hardware cell library a hardware cell for performing the desired function of the desired ASIC through application of the rules; and generating a netlist that identifies the hardware cells needed to perform the function of the desired ASIC and the necessary parameters for connecting the respective inputs and outputs of each hardware cell, the netlist is passed to the next subsequent step in the process for manufacturing the desired ASIC. ("netlist"= a description of the hardware components	Synopsys and Defendants provide their constructions for the disputed claim terms, phrases, and clauses and support for these two separate "selecting" and "generating for the selected integrated hardware cells" steps below and separately for each step. Synopsys and Defendants dispute Ricoh's attempt to improperly and misleadingly combine these two separate steps.

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base and generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor.	(and their interconnections) needed to manufacture the ASIC as used by subsequent processes, e.g., mask development, foundry, etc.) <u>Support</u> '432 Patent: Figs. 4, 9, 13; column 1, lines 17-26; column 2, lines 34-36; column 2, lines 42-44; column 5, lines 25-29; column 5, lines 35-40; column 8, lines 21-23; column 8, lines 26-41; column 8, lines 58-64; column 9, lines 8-24; column 9, line 64 to column 10, line 7; column 10, lines 13-34; column 13, line 36 to column 14, line 6. RCL000207-223, RCL000229-237. "expert system": (1977): computer software that attempts to mimic the reasoning of a human specialist. Merriam-Webster's Collegiate Dictionary Tenth Edition (1999). RCL011408-410 at RCL011410. "interconnection": To connect with one another. Merriam-Webster's Ninth New Collegiate Dictionary (1987). RCL011389-407 at RCL011403.	

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
	"requirement": Something wanted or needed-Necessity. Merriam-Webster's Ninth New Collegiate Dictionary (1987). RCL011389-407 at RCL011404.	
selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit, said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert	See the "selecting" row at column 2, *supra*, for Ricoh's analysis of this claim element. Because the selecting step was amended to include (and was granted as including) both "applying" and "generating" substeps, Ricoh has interpreted this claim element as a single claim element. Ricoh believes that Synopsys and the ASIC Defendants' attempt to cull out the "generating" substep as a separate and distinct claim element is an improper rewriting of the claim.	N. "selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit" -- mapping the specified stored definitions for each logical step and decision represented in the flowchart to a corresponding stored hardware cell description. *Intrinsic Evidence:* **'432 patent:** Fig. 4; 3:16-19; 4:66-5:3; 5:22-29; 8:31-37; 8:58-60; 9:52-60; 16:34-65 [Attachment 2, DEF012564-DEF012585]; **'432 patent file history:** April 1989 Amendment at 10 [Attachment 3, DEF011820-DEF012110]. *Extrinsic Evidence:* **Decl. Kowalski** ¶ 55. O. "said step of selecting a hardware cell comprising applying to the specified definition of the action

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
system knowledge base and		or condition to be performed, a set of cell selection rules stored in said expert system knowledge base" -- the mapping of the specified definitions to the stored hardware cell descriptions must be performed by an expert system having an inference engine for selectively applying a set of rules, each rule having an antecedent portion (IF) and a consequent portion (THEN), embodying the knowledge of expert designers for application specific integrated circuits, which enables the expert system to map the specified stored definitions for each logical step and decision represented in the flowchart to a corresponding stored hardware cell description. *Intrinsic Evidence:* **'432 patent:** Abstract; 2:58-63; 5:6-8; 8:29-37; 8:58-60; 9:8-13; 11:16-26; 16:34-65 [Attachment 2, DEF012564-DEF012585]; **'432 patent file history:** April 1989 Amendment at 8-11, 17; October 1989 Examiner Interview Summary; November 1989 Amendment at 4, 6-7, 9 [¶¶ Attachment 3, DEF011820-DEF012110]; **'435 patent**: 7:32-9:35[Attachment 4, DEF012503-DEF012518]; **'603 patent:** at 3:59-63 [Attachment 6, DEF017456-DF017482]; **'016 patent:** 3:5-8; 9:67-10:2, [Attachment 5,

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
		DEF017265-DEF017284; **An Overview of Logic Synthesis Systems:** at 170 [Attachment 7, DEF011962-DEF011968]; **The CMU Design Automation System:** at 75-77 [Attachment 8 , DEF012045-DEF012052]. *Extrinsic Evidence:* **Decl. Kowalski** ¶¶ 56-57 Same as set forth for phrases H, I, & J above. *Dictionaries, Treatises, Textbooks, etc.* Same as set forth for phrases H, I & J above.

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor.	See the "selecting" row at column 2, *supra*, for Ricoh's analysis of this claim element. Because the selecting step was amended to include (and was granted as including) both "applying" and "generating" substeps, Ricoh has interpreted this claim element as a single claim element. Ricoh believes that Synopsys and the ASIC Defendants' attempt to cull out the "generating" substep as a separate and distinct claim element is an improper rewriting of the claim.	P. "Netlist" -- a structural description that includes a custom controller type hardware cell and all other hardware cells required to implement the application specific integrated circuit's operations and any necessary interconnections including the necessary control and data path information for connecting the hardware cells and the controller. *Intrinsic Evidence:* **'432 patent:** Abstract; 1:17-37; 2:39-44; 4:39-43; 5:8-12; 5:30-40; 9:62-10:9; 12:31-35; 13:55-14:3; 16:34-65 [Attachment 2, DEF012564-DEF012585]. *Extrinsic Evidence:* **Decl. Kowalski** ¶¶ 58-60. Q. "generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit" -- producing a list of the needed hardware cells by eliminating any mapped hardware cells that are redundant or otherwise unnecessary and producing a custom controller type hardware cell for providing the needed control for those other hardware cells and

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
		Intrinsic Evidence: **'432 patent:** Abstract; 1:17-37; 2:39-44; 4:39-43; 5:8-12; 5:30-40; 9:62-10:9; 13:55-14:3; 16:34-65 [Attachment 2, DEF012564-DEF012585]. *Extrinsic Evidence:* **Decl. Kowalski** ¶¶ 61-62. R. "generating …interconnection requirements therefor" -- producing the necessary structural control paths and data paths for the needed hardware cells and the custom controller. *Intrinsic Evidence:* **'432 patent:** Abstract; Figs. 6 & 13-15; 1:17-37; 2:39-44; 3:23-25; 3:40-45; 4:39-43; 5:8-12; 5:30-40; 9:62-10:9; 13:55-14:3; 16:34-65 [Attachment 2, DEF012564-DEF012585]. *Extrinsic Evidence:* **Decl. Kowalski** ¶¶ 63-64.
14. A process as defined in claim 13, including generating from the netlist the mask data required to	The process of claim 13, including producing from the netlist of hardware cells to be included in the designed ASIC mask data which can be directly used by a chip foundry in the fabrication of the ASIC.	S. "generating from the netlist the mask data required to produce an integrated circuit having the desired function" -- producing, from the structural netlist, the detailed layout level geometrical information required for

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
produce an integrated circuit having the desired function.	Support '432 Patent: Figs. 1c, 2; column 1, lines 42-43; column 2, lines 44-49; column 3, line 68 to column 4, line 4; column 4, lines 44-46; column 5, lines 40-46.	manufacturing the set of photomasks that are used by the processes that directly manufacture the application specific integrated circuit. *Intrinsic Evidence:* **'432 patent:** Abstract; Fig. 1c; 1:42-44; 1:54-58; 2:44-49; 4:44-46; 5:40-46; 14:4-6; 16:34-68 [Attachment 2, DEF012564-DEF012585]; **'016 patent:** 1:41-47; 1:57-61; 4:11-13 [Attachment 5, DEF017265-DEF017284]. *Extrinsic Evidence:* **Decl. Kowalski** ¶¶ 65-66.
15. A process as defined in claim 13 including the further step of generating data paths for the selected integrated circuit hardware cells.	The process of claim 13, including producing signal lines for carrying data to the hardware cells. Support '432 Patent: Figs. 11, 13; column 2, lines 39-40; column 3, lines 60-65. RCL000207-223.	T. "generating data paths for the selected integrated circuit hardware cells" -- producing the necessary structural descriptions of the data paths for the mapped hardware cells. *Intrinsic Evidence:* **'432 patent:** Abstract; 2:39-40; 4:63-66; 5:6-12; 5:30-37; 6:29-31; 6:37-43; 6:50-53; 9:62-10:9; 13:55-14:3; 16:34-65; 17:1-3 [Attachment 2, DEF012564-DEF012585]; **'016 patent:** 2:21-25 [Attachment 5, DEF017265-017284]. *Extrinsic Evidence:*

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
		Decl. Kowalski ¶¶ 67-69. *Dictionaries, Treatises, Textbooks, etc.:* **IEEE Standard Dictionary** at 898 [Attachment 19, DEF085344-DEF085347].
16. A process as defined in claim 15 wherein said step of generating data paths comprises applying to the selected cells a set of data path rules stored in a knowledge base and generating the data paths therefrom.	The process of claim 15, wherein the step of producing signal lines for carrying data comprises applying rules, which are placed in computer memory, to produce the signal lines for carrying data to the hardware cells. Support '432 Patent: Column 4, lines 64-66. RCL000207-223.	U. "said step of generating data paths comprises applying to the selected cells a set of data path rules stored in a knowledge base and generating the data paths therefrom" -- the generating step must be performed by at least an expert system having an inference engine for selectively applying a set of rules, each having an antecedent portion (IF) and a consequent portion (THEN), embodying the knowledge of expert designers for application specific integrated circuits, which enables the expert system to produce the necessary data paths for the mapped hardware cells. *Intrinsic Evidence:* **'432 patent:** Abstract; 5:6-12; 9:62-10:9; 13:55-14:3; 16:34-65; 17:1-7 [Attachment 2, DEF012564-DEF012585]; **'432 patent file history:** April 1989 Amendment at 11 [Attachment 3, DEF011820-DEF012110]; **'435 patent**: 7:32-9:35 [Attachment 4, DEF012503-DEF012518]; **An Overview of Logic Synthesis**

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
		Systems: at 170 [Attachment 7, DEF011962-DEF011968]; **The CMU Design Automation System:** at 75-77 [Attachment 8, DEF012045-DEF012052. *Extrinsic Evidence:* **Decl. Kowalski** ¶¶ 69-70. Same as set forth for phrases H, I, & J above. *Dictionaries, Treatises, Textbooks, etc.* Same as set forth for phrases H, I & J above.
17. A process as defined in claim 16 including the further step of generating control paths for the selected integrated circuit hardware cells.	The process of claim 16, including producing signal lines for carrying control signals to the hardware cells. Support '432 Patent: Figs. 11, 13; column 2, lines 40-42; column 3, lines 60-65. RCL000207-223.	V. "generating control paths for the selected integrated circuit hardware cells" --producing the necessary structural descriptions of the control paths for the selected hardware cells. *Intrinsic Evidence:* **'432 patent:** Abstract; Figs. 1b & 13-15; 1:17-37; 2:40-42; 3:59-65; 4:39-43; 4:63-65; 5:3-12; 5:30-36; 6:18-27; 11:49-51; 13:51-14:3; 16:34-65; 17:1-10 [Attachment 2, DEF012564-DEF012585]; **'432 patent file history:** April 1989 Amendment at 8 [Attachment 3, DEF011820-DEF012110]; **'016 patent:** 2:20-24 [Attachment 5, DEF017265-DEF017284].

Claim Element	Ricoh's Construction(s) And Support For Those Construction(s)	Synopsys' & Defendants' Construction(s) And Support For Those Construction(s)
		Extrinsic Evidence: **Decl. Kowalski** ¶¶ 71-72. *Dictionaries, Treatises, Textbooks, etc.:* **IEEE Standard Dictionary** at 898 [signal line], [Attachment 19, DEF085344-DEF085347].

EXHIBIT 7

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX INCORPORATED, et al., Defendants.	Case No. C03-04669 MJJ (EMC) Case No. C03-2289 MJJ (EMC) **RESPONSIVE CLAIM CONSTRUCTION BRIEF FOR U. S. PATENT NO. 4,922,432 (RE-FILED)**
SYNOPSYS, INC., Plaintiff, vs. RICOH COMPANY, LTD., a Japanese corporation Defendant.	Date: October 29, 2004 Time: 9:30 AM Courtroom: 11 Judge: Martin J. Jenkins

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I. INTRODUCTION

Long-standing precedent from the Court of Appeals for the Federal Circuit prohibits patent owners, like Ricoh, from proffering interpretations for the purposes of litigation that would alter the indisputable public record and treat the claims as a "nose of wax." This is precisely what Ricoh seeks to accomplish here. Ricoh proffers interpretations for the disputed claim terms that contradict the clear import of the '432 patent, its file history, and the prior art that was distinguished from the invention in that file history.

For example, the public record for the '432 patent clearly and unmistakably limits the claimed invention by requiring that: (1) the input specifications be in a simple flowchart format; (2) the input specifications exclude what are known as register-transfer level descriptions; and (3) a rule-based expert system software be used as opposed to conventional software programs to select the hardware cells for the design of the desired ASIC. Because Ricoh knows that the use of the Synopsys Design Compiler® products at issue in the captioned actions are not capable of meeting any of these three requirements, Ricoh proposes constructions for the disputed claim terms that are contrary to the '432 patent's public record.

In fact, litigation induced interpretations that run contrary to the understanding of a person of ordinary skill in the art pervade Ricoh's entire opening claim construction brief. For this reason, the court should adopt Synopsys' and Defendants' proposed constructions, which are consistent with how a person of skill in the art would understand the '432 patent's claims, specification, and its file history.

II. LEGAL PRINCIPLES GOVERNING CLAIM CONSTRUCTION

The proper construction of disputed terms in a patent claim—*i.e.*, claim construction—is an issue of law reserved exclusively for the Court. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 372 (1996). Claim construction is the judicial determination of what is and what is not covered by the disputed terms in the patent claims. *Netword, LLC v. Centraal Corp.*, 242 F.3d 1347, 1352 (Fed. Cir. 2001) (citing *United States Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997)). Claim construction issues are legal issues for the Court to decide, and therefore, neither party bears the burden of proof on those legal issues.

Recently, the Court of Appeals for the Federal Circuit, in *Phillips v. AWH Corp.*, 376 F.3d 1382 (Fed. Cir. 2004) issued an order granting a petition to rehear that appeal, *en banc*, to address and resolve issues concerning claim construction. Specifically, that order demonstrates that the Federal Circuit will be addressing, *en banc*, issues regarding claim construction methodologies and the appropriate role and use of intrinsic evidence and extrinsic evidence such as expert testimony and technical dictionaries to interpret disputed claim terms. *Id*. at 1383-84. Despite the existing uncertainty in the Federal Circuit's decisions regarding the appropriate "methodology" for interpreting disputed claim terms, as recognized by the Federal Circuit's order in *Philips*, Synopsys and Defendants believe that the following five basic long-standing legal principles, explained below, should guide this court's construction of the disputed claim terms in the present action.

A. Disputed Claim Terms Are Generally Given Their Ordinary Meaning To One Of Ordinary Skill In The Art

When construing disputed claim terms, "the court must apply the same understanding as that of persons knowledgeable in the field of the invention." *Merck & Co v. Teva Pharms. USA, Inc.*, 347 F.3d 1367, 1371 (Fed. Cir. 2003) "'[P]atents are written not for laymen, but for and by persons experienced in the field of the invention.'" 347 F.3d at 1371 (citation omitted); *See also, Multiform Desiccants, Inc., v. Medzam, Ltd.*, 133 F.3d 1473, 1477 (Fed. Cir. 1998). "Accordingly, a technical term used in a patent is interpreted as having the meaning a person of ordinary skill in the field of the invention would understand it to mean." *Bell Atl. Network Servs. v. Covad Communications Group, Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). Generally, the court gives the disputed "claim terms their ordinary and accustomed meaning as understood by one of ordinary skill in the art." *Id.*[1]

"The ordinary and customary meaning of a claim term to one of ordinary skill in the art may

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[1] Some decisions from the Federal Circuit refer to a "presumption" of ordinary meaning for disputed claim terms—an issue of law. But Rule 301 of the Fed. R. Evid. provides that presumptions in civil actions "vanish[] upon the introduction of evidence sufficient to support a finding of the nonexistence of the presumed **fact**." *A.C. Aukerman Co. v. R.L. Chaides Constr. Co.*, 960 F.2d 1020, 1037 (Fed. Cir. 1992) (en banc) (emphasis added). Given that presumptions relate to "factual" and not "legal" issues, these cases merely stand for the proposition that claim terms should generally be given their ordinary meaning to a person of skill in the art unless the intrinsic evidence clearly supports (explicitly or implicitly) a different meaning.

be ascertained from a variety of sources . . .” *W.E. Hall Co. v. Atlanta Corrugating*, LLC, 370 F.3d 1343, 1350 (Fed. Cir. 2004). Such sources include: 1) the intrinsic evidence, *i.e.*, the patent’s claims, specification, and its file history, including any prior art cited in the patent or file history; and, 2) extrinsic evidence, such as expert testimony, technical dictionaries, treatises, and textbooks, and prior art not cited in the patent or its file history. *See id*; *Merck & Co.*, 347 F.3d at 1372; *Kumar v. Ovonic Battery Co.*, 351 F.3d 1364, 1368 (Fed. Cir. 2003). While extrinsic evidence may be useful to shed light on the relevant art and therefore assist the court in placing itself in the shoes of one of ordinary skill in the art, it is the intrinsic evidence that constitutes the public record of the patentee’s claim, a record on which reasonable competitors are entitled to rely. *See Vanderlande Indus. Nederland BV v. ITC*, 366 F.3d 1311, 1318 (Fed. Cir. 2004) (citing *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)).

B. Intrinsic Evidence Is The Most Significant Source For Determining The Ordinary Meaning Of Disputed Claims Terms

“‘It is well-settled that, in interpreting an asserted claim, the court should look first to the intrinsic evidence of record, *i.e.*, the patent itself, including the claims, the specification and, if in evidence, the prosecution history . . . Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language.’” *Bell Atl. Network Servs.*, 262 F.3d at 1267 (quoting, *Vitronics Corp.*, 90 F.3d at 1582).

First, the claim construction analysis always begins with the words of the claims, which are examined through the viewing glass of a person of skill in the art. *Interactive Gift Express, Inc. v. Compuserve, Inc.*, 256 F.3d 1323, 1331-32 (Fed. Cir. 2001); *See Vitronics*, 90 F.3d at 1582. While the focus may be on the particular claim terms or phrases in dispute, the “context of the surrounding words in a claim also must be considered in determining the ordinary and customary meaning of a disputed claim limitation.” *Arlington Indus., Inc. v. Bridgeport Fittings, Inc.*, 345 F.3d 1318, 1325 (Fed. Cir. 2003). In fact, the words in both the asserted and nonasserted claims must be considered in defining the scope of the claimed invention. *Vitronics*, 90 F.3d at 1582. Most importantly, in construing the disputed claim terms, “the analytical focus must begin and remain centered on the

language of the claims themselves, for it is that language that the patentee chose to use to 'particularly point[] out and distinctly claim[] the subject matter which the patentee regards as his invention.'" *Interactive Gift Express*, 256 F.3d at 1331 (quoting 35 U.S.C. § 112, ¶ 2).

Second, "'[c]laims are not interpreted in a vacuum, but are part of and are read in light of the specification.'" *Microsoft Corp. v. Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1347 (Fed. Cir. 2004) (citation omitted). "A fundamental rule of claim construction is that terms in a patent document are construed with the meaning with which they are presented in the patent document." *Merck & Co.*, 347 F.3d at 1371 ("[C]laims must be construed so as to be consistent with the specification, of which they are a part."). "Thus, the specification is always highly relevant to the claim construction analysis." *Vitronics*, 90 F.3d at 1582. "Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Id.* In short, the patent's description in the specification is always relevant to determining the ordinary and customary meaning of the disputed claim terms and therefore, must be examined for that purpose in every case.

Third, although "[t]he best source for understanding a technical term is the specification from which it arose," that understanding should be "informed, as needed, by the prosecution history." *Multiform Desiccants*, 133 F.3d at 1478. The prosecution history "reveals how those closest to the patenting process – the inventor and the patent examiner – viewed the subject matter." *Id.* Thus, the patent's file history is certainly a significant source for ascertaining the ordinary meaning of claim terms that must be reviewed in every case. *Jansen v. Rexall Sundown, Inc.*, 342 F.3d 1329, 1333 (Fed. Cir. 2003).

Besides the patent's claims, specification and its file history, the prior art cited in the patent and its file history also constitutes intrinsic evidence that provides valuable guidance that may be dispositive on the ordinary meaning of a claim term to one of skill in the art. *Kumar*, 351 F.3d at 1368. "'[W]hen prior art that sheds light on the meaning of a term is cited by the patentee, it can have particular value as a guide to the proper construction of the term, because it may indicate not only the meaning of the term to persons skilled in the art, but also that the patentee intended to adopt that meaning.'" *Kumar*, 351 F.3d at 1368 (quoting *Arthur A. Collins, Inc. v. N. Telecom, Ltd.*, 216 F.3d 1042, 1045 (Fed. Cir. 2000)). Thus, like the patent's claims, specification, and its file history,

the prior art cited in the patent or its file history is part of the intrinsic evidence and therefore, must also be examined for determining the ordinary meaning of claim terms in every case. *See Kumar,* 351 F. 3d 1368.

C. Extrinsic Evidence May Be Relied On To Ascertain The Ordinary Meaning Of Disputed Claims Terms

Extrinsic evidence may be examined by the court to help understand the disputed claim term, shed light on the relevant field of the invention, and ensure that the court's construction of the disputed claim terms are consistent with the "'clearly expressed, plainly apposite, and widely held understandings in the pertinent technical field." *AFG Indus., Inc. v. Cardinal IG Co., Ltd.*, 239 F.3d 1239, 1249 (Fed. Cir. 2001) (citations omitted); *See also, Vitronics*, 90 F.3d at 1584 ("extrinsic evidence…may be used only to help the court come to the proper understanding of the claims . . ."). Thus, extrinsic evidence may be used to assist the court in ascertaining the ordinary meaning of the disputed claim terms. *Bell Atl. Network*, 262 F.3d at 1268-69.

1. Prior Art, Technical Dictionaries And Treatises Are The Preferred Sources Of Extrinsic Evidence

Because prior art and technical dictionaries "are more objective and reliable guides" and such "sources are accessible to the public in advance of litigation", they are the extrinsic evidence sources that are preferred over expert opinion testimony. *Vitronics*, 90 F.3d at 1585. Specifically, "prior art can often help to demonstrate how a disputed term is used by those skilled in the art" and "may also be more indicative of what all those skilled in the art generally believe a certain term means." *Id*. at 1584. Similarly, the court may use technical dictionaries and treatises "to better understand the technology" and "when construing claim terms," as long as those definitions do not "contradict any definition found in or ascertained by a reading of the" intrinsic evidence. *Id*. at 1584 n.6. Thus, the court may certainly rely on both prior art not cited in the intrinsic evidence and technical dictionaries to ascertain the ordinary meaning of disputed claim terms. *Id*. at 1584-85.

2. **Non-Scientific Or General-Usage Dictionaries Are Irrelevant To The Meaning Of Terms Of Art And Ordinary Words Used In A Technological Context**

Unlike appropriate technical dictionaries and treatises reflecting the understandings of persons of skill in the field of the invention, however, except for limited circumstances, non-scientific or general-usage dictionaries are irrelevant to the meaning of both ordinary words "in a technological context" and technical terms of art in the field of the invention. *AFG Indus.*, 239 F.3d at 1248. "Only when the context is unclear, or it appears that the term is not being used in a technical manner, should the trial court rely upon a general purpose dictionary for construing the term." *Id.* "But where evidence – such as expert testimony…or technical dictionaries – demonstrates that artisans would attach a special meaning to a claim term, or…would attach no meaning at all to that claim term (independent of the specification), general-usage dictionaries are rendered irrelevant with respect to that term; a general-usage dictionary cannot overcome credible art-specific evidence of the meaning or lack of meaning of a claim term." *Vanderlande*, 366 F.3d at 1321. For these reasons, the Federal Circuit has repeatedly "'cautioned against the use of non-scientific dictionaries, 'lest dictionary definitions . . . be converted into technical terms of art having legal, not linguistic significance.'" *See e.g., id.* (citations omitted).

3. **Expert Testimony Should Be Used To Inform The Court's Construction And A Failure To Take Into Account Such Testimony May Constitute Reversible Error**

Although prior art (not cited in the intrinsic evidence) and technical dictionaries and treatises are the preferred sources of extrinsic evidence, expert testimony may also be used "to help the court come to the proper understanding of the claims." *Vitronics*, 90 F.3d at 1584. In fact, because a term of art must be construed in a manner consistent with the scientific and technical context in which it is used in the patent, in some instances "'the testimony of scientific witnesses is indispensable to a correct understanding' of the meaning of disputed claim terms, and . . .'it would undoubtedly be error for the court to reject the testimony.'" *AFG Indus., Inc.*, 239 F.3d at 1249 (quoting *Seymour v. Osbourne*, 78 U.S. 516, 546 (1871)). Expert testimony "can and should be used to inform the court's" construction of disputed claim terms and a "failure to take into account the testimony of

persons of ordinary skill in the art may constitute reversible error." *Id.* In short, where the claims contain technical terms or terms of art it is not only appropriate but preferable that the court consult trustworthy expert testimony to aid the court in coming to the correct conclusion on the proper meaning of disputed terms of art in the claims. *See id*.

D. Only Intrinsic Evidence May Be Used To Establish A Meaning For A Disputed Claim Term Other Than Its Ordinary Meaning To One Of Skill In The Art

Generally, the court gives the disputed "claim terms their ordinary and accustomed meaning as understood by one of ordinary skill in the art." *Bell Atl. Network*, 262 F.3d at 1267; *Vitronics*, 90 F.3d at 1582. The circumstances where a claim term may be construed to have a meaning other than its ordinary meaning to one of skill in the field of the invention include where the intrinsic evidence: 1) plainly defines the claim term either explicitly or by implication; 2) shows that the patentee distinguished the invention from a prior art reference, expressly disclaims subject matter from the scope of the invention, or highlights a particular feature as important to the invention; 3) provides meaning to a claim term that would otherwise render the scope of the claim unclear. *See e.g., W.E. Hall Co.*, 370 F.3d at 1353. The circumstances where a court's construction may depart from the ordinary meaning of a disputed claim term are best understood through examples of actual decisions.

1. The Intrinsic Evidence May Implicitly Define A Claim Term With Or Without An Explicit Statement Of Redefinition

First, a claim term may be redefined by the intrinsic evidence with or without an explicit statement of redefinition. *Bell Atl. Network*, 262 F.3d at 1268; *see, Vitronics*, 90 F.3d at 1584 n.6 (meaning of claim terms may be "'found in or ascertained by a reading of the patent documents'"). In *Bell Atl. Network*, the Federal Circuit affirmed the district court's grant of summary judgment of non-infringement. 262 F.3d at 1262. The Federal Circuit agreed with the district court's construction of the claim term "mode" because it was implicitly defined in the intrinsic evidence to be limited to the three broad categories described in the patent's specification. *Id*. at 1273. The Federal Circuit came to this conclusion in spite of the broad ordinary meaning of the non-technical term "mode." *Id*. at 1270. The reasoning behind the Federal Circuit's conclusion is that "a claim term may be clearly redefined without an explicit [definition]" and that "when a patentee uses a claim term throughout the

entire patent specification, in a manner consistent with only a single meaning, he has defined that term 'by implication.'" *Id.* at 1271 (citing *Vitronics*, 90 F.3d at 1582).

The Court also agreed with the district court's conclusion that even claims not explicitly reciting the "mode" limitation were also limited to the three broad categories described in the patent's specification. 262 F.3d at 1275. This conclusion was based on the Court's recognition that "one of ordinary skill in the art would understand that the transceiver" described in the claim not including the "mode" limitation was the same as the one that included the "mode" limitation and was therefore limited by the implicit definition of the term "mode" in the intrinsic evidence. *Id.*

2. The Patent's File History Limits The Invention By Excluding What Was Disclaimed

Second, the "doctrine of prosecution disclaimer is well established in Supreme Court precedent" and that doctrine has been adhered to by the Court of Appeals for the Federal Circuit "as a fundamental precept" in its "claim construction jurisprudence." *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1323 (Fed. Cir. 2003). Prosecution disclaimer refers to the Federal Circuit precedent that "the prosecution history limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution." *See e.g., Southwall Techs., Inc v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995) ("sputter-deposited dielectric" limited to one-step process by patentee's argument that dielectric was "directly deposited.").

"As a basic principle of claim interpretation, prosecution disclaimer promotes the public notice function of the intrinsic evidence and protects the public's reliance on definitive statements made during prosecution." *Omega Eng'g*, 334 F. 3d at 1324. "[F]or prosecution disclaimer to attach [Federal Circuit] precedent requires that the alleged disavowing actions or statements made during prosecution be both clear and unmistakable." *Id.* at 1325-6. In determining whether prosecution disclaimer limits the scope of the claimed invention, a court must assess "whether a patentee relinquished a particular claim construction based on the totality of the prosecution history, which includes amendments to claims and arguments made to overcome or distinguish references." *Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1326 (Fed. Cir. 2002); *See also, Biogen, Inc. v. Berlex Labs, Inc.*,

318 F.3d 1132, 1139 (Fed. Cir. 2003) (district court correctly found that based on examiner's statements "single DNA construct" limitation was basis on which all claims were allowed by examiner and properly declined to interpret "method claims as free of this limitation").

In *Biogen*, the Federal Circuit affirmed the district court's granting of the defendant's motion for summary judgment of non-infringement. 318 F.3d at 1142. The principle issue on appeal was whether the district court's interpretation properly limited the method claims to the use of a "single DNA construct" even though those method claims were not amended and did not mention the use of a "single DNA construct." *Id*. at 1134. The Federal Circuit agreed with the district court's conclusion that the examiner's statements after a telephonic interview with the applicant in the examiner's Reason for Allowance, read objectively, establishes that the "single DNA construct" was the examiner's only basis for allowing all of the claims. *Id*. at 1139. Thus, even the method claims that were not amended to include such a limitation were properly limited to the use of a "single DNA construct." *See e.g., ACCO Brands, Inc. v. Micro Sec. Devices, Inc.*, 346 F.3d 1075, 1079 (Fed. Cir. 2003) ("'[I]t is incorrect to construe a claim as encompassing the scope that was relinquished in order to obtain allowance of another claim, despite a difference in words used.'") (quoting *Modine Mfg. Co. v. United States Int'l Trade Comm'n*, 75 F.3d 1545, 1551 (Fed. Cir. 1996) (emphasis added) abrogated on other grounds by *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd.*, 234 F.3d 558 (Fed. Cir. 2000); *See also, Springs Window Fashions LP v. Novo Indus., L.P.*, 323 F.3d 989, at 995-6 (Fed. Cir. 2003) (distinguishing prior art patent limited claim scope to distinguishing features despite fact those features were not and are not reflected in claims).

Similarly, in the Federal Circuit's *ACCO Brands* decision, which also affirmed the granting of summary judgment of non-infringement by the district court, the Court concluded that the "pin clause" of unamended "claim 10 must be construed in the same way" as the amended "pin clause of claim 1." *ACCO Brands*, 346 F.3d at 1079. The Court came to this conclusion based on the statements in the examiner's Reasons for Allowance. *Id.* Those statements repeated the arguments presented by the applicant and demonstrated "that the examiner and the applicant understood that the invention requires that the pin extends (actively) into the slot after rotation." *Id.* The Court reasoned that although the pin clause of claim 10 was not amended and therefore, used different words for the

pin clause than the words used in amended claim 1, claim 10 could not be construed to encompass the subject matter that was relinquished to obtain claim 1. *Id.*

3. **The Patent's Specification May Also Limit The Scope Of The Invention**

"Whether an invention is fairly claimed more broadly than the 'preferred embodiment' in the specification is a question specific to the content of the specification, the context in which the embodiment is described, the prosecution history, and if appropriate the prior art, for claims should be construed, when feasible, to sustain their validity." *Wang Labs., Inc. v. Am. Online, Inc.*, 197 F.3d 1377, 1383 (Fed. Cir. 1999). "The usage 'preferred' does not of itself broaden the claims beyond their support in the specification." *Id*; *Bell Atl. Network*, 262 F.3d at 1273; *See also, Biogen*, 318 F.3d at 1140 (Claims do not "'enlarge what is patented beyond what the inventor has described as [his] invention.'") (quoting *Network*, 242 F.3d at 1352).

In *Biogen*, the Court agreed with the district court's conclusion "that the specification defines the invention as the use of a single DNA construct . . . and that the method and cell line claims, as well as the construct claims, are so limited." 318 F. 3d at 1140. The Court recognized that although the specification mentioned other known general techniques, the "specification does not describe or present details of any other configuration for introducing these genes" but instead "describes only linked DNA sequences and transformation procedures using single constructs . . . " *Id.* at 1136-37. The Court noted that the claims may not "'enlarge what is patented beyond what the inventor has described as [his] invention.'" *Id.* at 1140 (quoting *Network*, 242 F. 3d at 1352). The Court concluded that the district court's interpretation properly limited the method claims to the use of a "single DNA construct" even though those methods claims were not amended and did not mention the use of a "single DNA construct."

Similarly, in *Wang Labs*, the Federal Circuit agreed with the district court's conclusion that although the general usage of the term "frame" encompassed both bit-mapped display systems and character-based systems, the description in the patent of character-based systems limited the claimed invention to character-based systems. 197 F.3d at 1381. In that case, the Federal Circuit affirmed the district court's grant of summary judgment to the defendants on the issue of infringement. 197 F.3d 1379. The only issue on appeal was whether the district court properly limited the interpretation of

the term "frame" to the "character-based protocols" described in the patent's specification. *Id.* at 1380.

The Court concluded that the only embodiment described in the patent's specification "is the character-based protocol, and the claims were correctly interpreted as limited thereto." *Id.* at 1383. In reaching this conclusion, the Court recognized that "in order to be covered by the claims…subject matter must be sufficiently described as the applicant's invention to meet the requirements of [35 U.S.C.] section 112. This requirement was not met as to protocols other than character-based." *Id.* In other words, neither the mere mention of other protocols nor the usage of "preferred" in the patent changed the fact that the patent's description only supported character-based protocols. *Id.* at 1382.

Not only is the scope of the invention properly limited to what is supported by the patent's description, but the teachings in the patent's description "'about the problems solved by the claimed invention, the way the claimed invention solves those problems' and the prior art that relates to the invention'" all "'provide valuable context for the meaning of the claim language.'" *ResQNet.com, Inc. v. Lansa, Inc.*, 346 F.3d 1374, 1381 (Fed. Cir. 2003) (citations omitted). In fact, the patent's specification may certainly limit the claimed invention to important features that are essential for solving the problems in the prior art solved by the claimed invention. *See Gaus v. Conair Corp.*, 363 F.3d 1284, 1289-90 (Fed. Cir. 2004).

In *Gaus*, the Federal Circuit reversed the jury's verdict of infringement under the doctrine of equivalents and entered judgment of non-infringement for the defendant. *Id.* at 1285. The principle issue was whether the "double conductor" was required to be structurally separate from the "voltage-carrying electrical operating unit." *Id.* at 1289. The Court concluded that this "structural separation" was required because the specification demonstrated that this "separation" is how one of the principle advantages of the invention over the prior art was achieved. *Id.* at 1289-90. The Court specifically noted that even if the claim language did not support the adopted construction, the specification's description that the "structural separation" was necessary for achieving the inventions advantages over the prior art presents "'a clear case of disclaimer of subject matter.'" *Id.* at 1288 n.2 (citation omitted).

E. Extrinsic Evidence May Never Be Used To Alter A Claim Term's Ordinary Meaning Or Any Other Meaning Established In The Intrinsic Evidence

Extrinsic evidence may never be used to vary, contradict, expand, or limit any meaning found in or ascertained from the intrinsic evidence. *See e.g.*, *Omega Eng'g*, 334 F.3d at 1332 (citing *Vitronics*, 90 F.3d at 1584-85). In fact, "[i]f the meaning of the claim limitation is apparent from the intrinsic evidence, it is improper to rely on extrinsic evidence other than that used to ascertain the ordinary meaning of the claim limitation." *Id.* (citing *Vitronics*, 90 F.3d at 1582). This prevents a patentee from "proffer[ing] an interpretation for the purposes of litigation that would alter the indisputable public record . . . and treat the claims as a 'nose of wax.'" *Vitronics*, 90 F.3d at 1583 (quoting *Southwall*, 54 F.3d at 1578).

III. SUMMARY OF THE '432 PATENT

A. The Goal Of The '432 Patent's Alleged Invention Is To Enable Non-Experts To Design ASICs

The '432 patent explains that the "invention provides a computer-aided design system and method for designing an application specific integrated circuit . . . " (Ex. 1 at Abstract). "An application specific integrated circuit (ASIC) is an integrated circuit chip designed to perform a specific function, as distinguished from standard, general purpose integrated circuit chips, such as microprocessors, memory chips, etc." (*Id*. at 1:13-17). Unlike general-purpose integrated circuit chips such as microprocessors, which are designed so that they may execute software for performing many different applications, an ASIC is designed for a specific function, for example, to control the operation of a vending machine. (*Id.* at 12:39-44).

According to the '432 patent, the ASIC design processes of the prior art require the designer to consider the required objectives and tasks for the desired ASIC and define the structural level design specification for that ASIC. (Ex. 1 at 1:19-23). This structural level design specification (or netlist) must define the various hardware components and their required interconnections as well as a system controller for synchronizing the operations of those hardware components. (*Id*. at 1:23-27). Because defining structural level design specifications requires the ASIC designer to have an "extensive and all encompassing knowledge" of these hardware components and their required

interconnections, the '432 patent concludes that the ASIC design process requires engineers with highly specialized skills and expertise in VLSI design. (*Id.* at 1:28-32, 1:58-65).

The stated goal of the '432 patent's claimed invention is to enable non-expert designers (*i.e.*, designers not having highly specialized skills and expertise in VLSI design) to design ASICs. (Ex. 1 at 2:14-19). The '432 patent's invention purports to accomplish this goal with computer-aided design software that: 1) allows non-expert designers to work with "simple flowcharts" that they are able to understand and which only requires them to know what the necessary logical steps are to complete a task and, 2) provides and applies the essential VLSI design expertise needed to design ASICs through the use of a rule-based expert system "extracted from expert ASIC designers." (Ex. 1 at 2:24-27, 2:57-63; 4:5-34, *see also* Abstract)(emphasis added):

> The flowchart is a highly effective means of **describing a sequence of logical operations**, and is well understood by software and hardware designers of **varying levels of expertise** and training.
>
> * * *
>
> The KBSC utilizes a **knowledge based expert system**, with a knowledge base **extracted from expert ASIC designers** with a high level of expertise in VLSI design to **generate from the flowchart a netlist** . . .
>
> * * *
>
> [T]he **design of an integrated circuit** at the structural level **requires** a design engineer with **highly specialized skills and expertise in VLSI design**. In the KBSC system of the present invention, however, integrated circuits can be designed at a functional level **because the expertise in VLSI design is provided and applied by the invention**. Allowing the designer to work with flowcharts…simplifies the task of designing custom integrated circuits . . . The designer deals with an algorithm using **simple flowcharts**…and needs to know only the **necessary logical steps** to complete a task . . .
>
> * * *

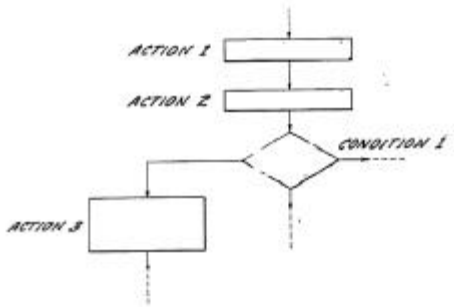
Thus, the "simple flowchart input" and the "rule-based expert system for generating a netlist from a flowchart" features are essential to achieving the '432 patent's stated goal. In fact, the '432 patent's inventor touted these same two essential features, *i.e.*, the "flowchart input form" and the "rule-based approach…to logic synthesis," as what he believed "clearly distinguished" his invention from existing prior art systems in an article around the same time of the '432 patent application. (Ex. 2 at 389).

B. Rule-Based Expert System Software For Translating A Flowchart Input To A Netlist Is The Only Embodiment Of The '432 Patent's Claimed Invention

There is only one embodiment of the system and method of the claimed invention described in the '432 patent and it is referred to as the Knowledge Based Silicon Compiler (also referred to herein as "KBSC"). (Ex. 1 at 2:50-53). As its name suggests, the Knowledge Based Silicon Compiler software is an ASIC design methodology based upon expert systems technology. (*Id*. at 2:53-55). Specifically, the KBSC software uses a flowchart editor to permit non-expert designers to represent the desired ASIC in a flowchart format and generates a netlist from that flowchart input using a rule-based expert system. (*Id*. at 2:55-62). More specifically, the only embodiment described in the '432 patent (the KBSC method) is an ASIC design method consisting of the following four basic steps described in detail in the following paragraphs.

1. ***Step One*: Using The Flowchart Editor of KBSC, The Non-Expert Designer Describes A Sequence Of Operations For The Target ASIC**

In the sole embodiment described in the patent, the first step for defining the flowchart input specification for the ASIC to be designed is for the non-expert designer to represent the sequence of logical operations (*i.e.*, actions and conditions) in a flowchart format using the flowchart editor 21. (Ex. 1 at 2:24-27). The flowchart editor is the user interface software program. It allows the user to display, create and edit flowcharts. (*Id.* at 4:56-59; 7: 6-7). Specifically, the flowchart editor 21 is used to create, edit, and delete the rectangles (actions), diamonds (conditions), and lines (transitions) in the flowchart to represent the series of logical steps and decisions needed to accomplish the task of the desired ASIC. (Ex. 1 at 2:24-27; 3:50-59; 4:15-19; 7:12-23; 8:51-56). The result of this step is shown in the following figure, which is taken from Figure 5 in the '432 patent.



2. ***Step Two*: Using The Flowchart Editor of KBSC, The Non-Expert Designer Specifies A Macro For Each Action And Condition Represented In The Flowchart**

Once the non-expert designer has represented the sequence (or series) of actions and conditions (*i.e.*, operations) for the desired ASIC in the flowchart, the second step in defining input specification for the ASIC to be designed is the designer's use of the flowchart editor to assign (*i.e.*, specify) a definition from the stored definitions (*i.e.*, Macro Library) for each of the actions (rectangles) and conditions (diamonds) represented in the flowchart. (Ex. 1 at 4:61-63; 5:20-22; 7:24-50; 8:23-26). Table 1 from the '432 patent shows a Macro Library containing the definitions for the available actions and conditions that may be specified in the flowchart. The result of this specifying step is shown in Figure 5 of the '432 patent.[2]

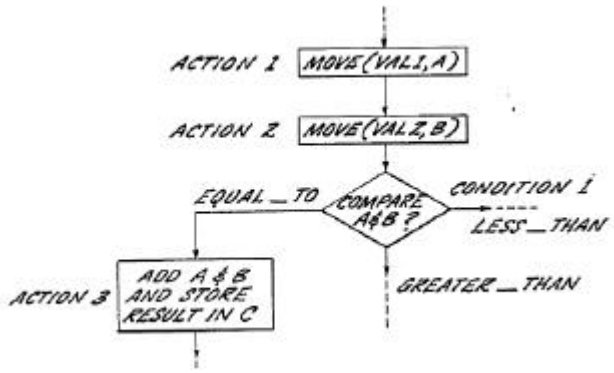


TABLE 1

Macro	Description
ADD (A,B,C)	C = A + B
SUB (A,B,C)	C = A − B
MULT (A,B,C)	C = A * B
DIV (A,B,C)	C = A div B
DECR (A)	A = A − 1
INCR (A)	A = A + 1
CLR (A)	A = 0
REG (A,B)	B = A
CMP (A,B)	Compare A to B and set EQ,LT,GT signals
CMP0 (A)	Compare A to 0 and set EQ,LT,GT signals
NEGATE (A)	A = NOT (A)
MOD (A,B,C)	C = A Modulus B
POW (A,B,C)	C = A B
DC2 (A,S1,S2,S3,S4)	Decode A into S1,S2,S3,S4
EC2 (S1,S2,S3,S4,A)	Encode S1,S2,S3,S4 into A
MOVE (A,B)	B = A
CALL sub-flowchart (A,B, . . .)	Call a sub-flowchart. Pass A,B . . .
START (A,B, . . .)	Beginning state of a sub-flowchart
STOP (A,B . . .)	Ending state of a sub-flowchart

After the definitions have been specified for each operation in the flowchart, as shown for example in Figure 5, the flowchart is then converted to an intermediate file, called a statelist. (Ex. 1 at 7:1-3; 8:56-57).[3]

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[2] Specifically, the ADD (A,B,C) definition from Table 1 is specified for ACTION 3 and the MOVE (A,B) definition from Table 1 is specified for ACTIONS 1 and 2. Similarly, the definition CMP (A,B) from Table 1 is specified for CONDITION 1.

[3] As explained further in Section II.C. below, the statelist is a list form description converted from the flowchart and an example statelist is shown in Appendix A of the '432 patent. (Ex. 1 at 14:7-30).

3. *Step Three*: The Rule-Based Expert System of KBSC Selects The Hardware Cell For Performing Each Definition Specified In The Flowchart

In this step, each definition assigned by the designer using the flowchart editor to each of the actions and conditions represented in the flowchart is matched by the cell selector software program of KBSC to an appropriate corresponding hardware cell description from a library of cells. (Ex. 1 at 5:20-25, 8:23-32):

> The selection is based on the functional descriptions in the flowchart, as specified by the macros assigned to each action represented in the flowchart. …To design a VLSI system from a flowchart description of a user application, it is necessary to match the functions in a flowchart with cells from a cell library.

The cell selector software program of KBSC maps the specified definitions to the hardware cell descriptions using a number of design parameters and constraints such as cell function, process technology used, time delay, power consumption, etc. (Ex. 1 at 8:26-29, 8:60-64, 9:52-61). This makes mapping each specified definition in the flowchart to the appropriate hardware cell description complicated. Consequently, the cell selector must use a rule-based expert system. (Ex. 1 at 5:25-29, 8:29-60):

> The cell selector uses a knowledge base extracted from VLSI design experts to make the cell selection. …This mapping needs the use of artificial intelligence techniques because the cell selection process is complicated…. The Cell Selector uses a rule based expert system to select the appropriate cell or cells to perform each action.

The rule-based expert system's mapping or matching of the specified definitions from the macro library to the hardware cell descriptions in the cell library is illustrated in Figure 4 of the '432 patent.

4. *Step Four*: The Rule-Based Expert System Generates A Netlist Defining The Necessary Hardware Cells And Their Required Interconnection

After the hardware cells have been selected by the rule-based expert system, the KBSC software generates the netlist. (Ex. 1 at 9:64-65). The netlist, as described in the '432 patent, must have all of the necessary hardware cells that are required to implement the designated operations of the ASIC. Thus, the netlist must include a custom controller type hardware cell as well as the data

paths and control paths necessary for connecting the selected hardware cells. (Ex. 1 at 2:34-44; 4:39-43; 5:30-37).

> The netlist 15 includes a custom generated system controller, all other hardware cells required to implement the necessary operations, and interconnection information for connecting the hardware cells and the system controller.

The KBSC software uses a rule-based expert system to generate the controller type hardware cell and the necessary control and data paths that form the required interconnections for all of the hardware cells. (Ex. 1 at Abstract, 5:8-12). After the controller and the data and control paths have been generated, the rule based expert system then eliminates selected hardware cells that are redundant or unnecessary (Ex. 1 at 13:59-66). Finally, the controller, the other necessary hardware cells, and the data and control paths for connecting those hardware cells are used to define the netlist for the desired ASIC. (Ex. 1 at 13:67-14:3).

C. The '432 Patent Does Not Describe A "List Form" Input Specification Embodiment

Ricoh, in its opening brief, claims that the single off-hand mention of a "list form" input in the '432 patent's specification and unasserted claim 2's unsupported requirement that the input means "a list defining the series of actions and conditions" by themselves constitute another described embodiment. (Ex. 1 at 2:21-24; 14:67-15:2). They do not.

The only "list" ever mentioned in the '432 patent is the intermediate file referred to as a statelist. The statelist is not user input, but rather is generated by the KBSC software from the input specification in the flowchart format. (Ex. 1 at 7:1-2, 8:56-57). The '432 patent does not provide any description of the statelist's format, but Appendix A is an example statelist. (*Id*. at 14:7-30).

The only description of this "list form" is provided in United States Patent No. 5,197,016 ("the '016 patent"), issuing from a continuation-in-part application which was filed 18 months later by the two inventors of the '432 patent. (Ex. 3). Specifically, the '016 patent describes an Antecedent-Action-Form ("AAF") that is converted from the input specification in the flowchart

format. (*Id*. at 7:33-9:53). The AAF file examples in the '016 patent are the same as Appendix A in the '432 patent. (Ex. 1 at 14:7-30 with Ex. 3 at 9:26-35 and 9:21-53).[4] Thus, the description in the '016 patent confirms that the only "list" in the '432 patent is not a separate input specific embodiment but is instead a "generated" interim file format.

D. **The '432 Patent Does Not Describe An Embodiment For Automatically Mapping The Stored Definitions**

Ricoh's proposed constructions for the "describing" and "specifying" steps improperly seeks to eliminate the second "specifying" step for defining the input specification for the ASIC to be designed. Specifically, Ricoh's proposed construction for the "describing" step appears to require that the input specification be completely defined in that "describing" step. But then, Ricoh's proposed construction for the "specifying" step confusingly and inconsistently suggests that the "macros may also be 'mapped' automatically." Ricoh's claim construction is contrary to the '432 patent's description because the "specifying" step is the second of the two steps for defining the input specification (*i.e.*, specifying the macros).[5]

To support its construction and oppose Synopsys' and Defendants' construction for the "specifying" step, Ricoh claims that Synopsys' and Defendants' proposal excludes a so-called embodiment where "macros may also be 'mapped' automatically through application of rules." Ricoh bases this claim solely on the following portion of the '432 patent describing the use of rules by the cell selector to generate a blocklist from the statelist. (Ex. 1 at 9:6-18) (Ricoh's quote shown underlined):

> Cell List Generation
>
> FIG. 9 shows the cell list generation steps. The first step of the cell list generation is the transformation of the flowchart description into a structure that can be used by the Cell Selector. This structure is called a statelist. The blocklist is generated from the statelist by

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[4] This description reveals that the AAF file format is nothing more than a descriptive list of the information provided in the flowchart that it was converted from.

[5] The KBSC software cannot define the ASIC to be designed. The designer must provide the specification for the ASIC. In other words, the designer (not the KBSC software) determines the input to the KBSC (*e.g.*, the ASIC design) by assigning the macros to the "series" of actions (rectangles) and conditions (diamonds) represented in the flowchart. The KBSC software is not capable of inferring the macro (specified definition) that should be specified for each rectangle or diamond in the flowchart.

> the inference engine. The blocklist contains a list of the functional blocks to be used in the integrated circuit. Rules of the following type are applied during this stage.
>
> map arguments to data paths
> map actions to macros
> connect these blocks

In its proper context, however, Ricoh's quote from the '432 patent description demonstrates that the "map actions to macros" rule type is applied during the generation of a blocklist containing functional blocks from the statelist. Moreover, the "connect these blocks" rule type in this portion of the specification demonstrates that the "macros" in the "map actions to macros" rule type refers to the functional blocks in the blocklist. Thus, Ricoh's assertion that there is an embodiment for "automatic mapping of stored definitions" is contrary to the '432 patent's description.

IV. THE '432 PATENT'S PROSECUTION HISTORY

A. The Original Application For The '432 Patent

The patent application which led to the issuance of the '432 patent was filed on January 13, 1988 with thirty claims (1-30). (Ex. 4, Original Application). The '432 patent claims 13-17 at issue here correspond to application claims 20-26 in the original application. (*Id.* at 34-36). Application claim 20, later amended to incorporate the limitations recited in application claims 21 and 25 corresponds to the issued claim 13, which is the only independent claim in the present litigation. (*Id.*). A year after the application was filed, on January 18, 1989, the examiner issued an office action rejecting all thirty of the pending claims in the application. (Ex. 4, January 1989 Office Action at 2).

B. The April 18, 1989 Amendment

In response to the examiner's January 13, 1989 rejection of all thirty pending claims, a completely new phrase "architecture independent" was added throughout the patent application in an attempt to distinguish the claimed invention over the prior art. (Ex. 4, April 1989 Amendment at 1-8). Specifically, the phrase "architecture independent" was added to the claims, the specification including the Summary of the Invention, and the Abstract of the Disclosure. (*Id.*). Prior to this amendment, the application described the claimed invention's input as a functional specification comprising a series of actions and conditions. (Ex. 4, Original Application at 30 (Claim 5)).

This amendment limits the '432 patent's claimed invention's input to "architecture independent" functional specifications comprising a series of architecture independent actions and conditions. (Ex. 4, April 1989 Amendment at 8). To distinguish the '432 patent's invention over the functional specifications in the Darringer et al. prior art, this amendment defines "architecture independent functional specifications" as functional specifications that exclude register-transfer level descriptions as defined in the Darringer et al. prior art patent. (*Id*. at 9) (emphasis added):

> A **very clear distinction** between Darringer and the present invention is that the **input to the Darringer system is in the form of a register transfer level flowchart control language**. Darringer et al., U.S. Patent No. 4,703,435, column 4, lines 26-32. …**In contrast**, the application specific circuit designer utilizing the present invention need not possess any expertise common among highly skilled VLSI design engineers since the **input to the present invention is in the form of an architecture independent functional specification**.

A register-transfer level description input by the user would specify the control at the clock cycle level for the ASIC to be designed. (Ex. 5 at 5:27-35). In contrast, the invention in the '432 patent generates a controller, which provides the clock cycle level control, from the described "sequence of operations" represented in the flowchart. (Ex. 4, April 1989 Amendment at 8; *See also*, Ex. 1 at 1:26-28; 2:39-41). Because of this, excluding a register-transfer level description input from the claimed invention is required for the only embodiment in the '432 patent to make sense. Moreover, as emphasized in the April 1989 Amendment, register-transfer level descriptions require the expertise of highly skilled VLSI designers, and therefore such descriptions cannot be encompassed by the '432 patent's claimed invention because they are contrary to its stated goal. (Ex. 4, April 1989 Amendment at 9, 13, 16).

The April 1989 Amendment also establishes that claim 13 requires the use of a rule-based expert system for selecting hardware cells from a hardware cell library. (Ex. 4, April 1989 Amendment at 9-10, 11; see also 17) (emphasis added):[6]

> While Darringer may **synthesize logic** from a register transfer level flowchart description, **it provides no knowledge base** of any kind. **In contrast**, the present invention, …provides **a knowledge base in the**

[6] Application claim 21 is incorporated into issued claim 13 in the November 1989 Amendment.

> **form of a rule based automatic logic synthesis component, *i.e.*, an expert system**. Thus, Darringer does not teach the method of synthesis utilized by the present invention. Furthermore, although it is known in the art of automatic layout to utilize hardware cell libraries, **a rule based expert system has not been utilized to accomplish a task of selection of cells** from the cell library.
>
> * * *
>
> **In contrast**, the present invention, **utilizes a knowledge base which consists of a rule based expert system to synthesize logic**….

Besides requiring the use of a rule-based expert system for selecting the hardware cells, this amendment and the original application also confirm that a rule-based expert system for selecting hardware cells is comprised of a knowledge base of rules for selecting hardware cells and an inference engine for applying those cell selection rules to select appropriate hardware cells from the hardware cell library. (*Id*; Ex. 4, Original Application, (claims 6 and 16) at 30 and 33).

Finally, the Dunn prior art patent demonstrates that rule-based expert systems are substantially different from conventional computer programs that use predefined algorithms. (Ex. 6 at 1:30-56). Specifically, this prior art patent shows that rule-based expert systems use inference methods for applying the rules that make up the knowledge in the field to a solve problems, whereas conventional software programs "solve problems in accordance with pre-defined algorithms and complete data sets." (*Id*.). Thus, this amendment also confirms the substantial differences between using the rule-based expert system software programs of the alleged invention and using the predefined algorithms of conventional software programs of the prior art.

C. **The October 19 1989 Examiner Interview Summary**

Despite the limiting amendments and arguments made by the applicant in the April 1989 Amendment, on August 15, 1989 in a Final Office Action, the examiner again rejected all thirty of the pending claims. (Ex. 4, August 1989 Office Action). As a result of this final rejection of all of the pending claims, the applicant and the examiner participated in an interview.

During that interview, the applicant and the examiner reached an agreement regarding the features of the '432 patent's claimed invention including claim 13 (application claim 20) that distinguished the claimed invention over the Darringer et al. prior art. (Ex. 4, Examiner Interview Summary Record). That agreement unmistakably limits the '432 patent's claimed invention's input

to a flowchart format. The agreement also unmistakably limits the '432 patent's claimed invention to the translation of that flowchart input to a netlist through the use of an expert system. (*Id.*) (emphasis added):

> It is **agreed** that the **features** "flowchart editor" and "expert system for translating the flowchart into a netlist defining the necessary hardware cells of the integrated circuit" are patentable [*sic*] distinct from the reference identified above. Thus, applicant's attorney **will** amend the claims to include **those features**.

The "flowchart editor" feature is the software module operable by a designer and provides the means for the designer to enter the architecture independent functional specification by performing the following two steps: 1) creating a flowchart having boxes representing actions, diamonds representing conditions, and lines with arrows representing the transitions between those actions and conditions; and 2) specifying for each box or diamond a particular action or condition from the available stored definitions (*i.e.*, the Macro Library). (Ex. 4, Original Application at 13:1-14:45, 16:29-17:4). Thus, the agreement reached by the applicant with the examiner without a doubt limited both the "describing" and "specifying" steps of claim 13 (application claim 20) to the use of a flowchart format.

D. **The November 15, 1989 Amendment**

Shortly after reaching the agreement with the examiner, on November 15, 1989, the applicant filed an amendment. (Ex. 4, November 1989 Amendment). In that amendment the applicant amended claim 13 (application claim 20) to incorporate the language of application claim 21 and to add the step of application claim 25. (Ex. 4, November 1989 Amendment at 4-5):

These amendments are consistent with the agreement reached between the applicant and the examiner. First, they limit the "selecting step" by requiring that it be done using a rule-based expert system. (Ex. 4, November 1989 Amendment at 7).

Second, they define the "expert system for translating" feature as a knowledge base containing the cell selection rules and an inference engine for applying those rules to select the appropriate hardware cells. (Ex. 4, November 1989 Amendment at 2, 8) (emphasis added):

> an expert system including a knowledge base containing rules for selecting hardware cells from said cell library and **inference engine** means for selecting appropriate hardware cells from said cell library in accordance with the rules of said knowledge base

* * *

> Claim 5 has also been amended to clearly distinguish it over the cited prior art by more clearly defining the expert system aspects of applicants' invention including the provision of a knowledge base containing rules for selecting hardware cells, [and] inference engine means for selecting appropriate hardware cells . . .

Third, the amendment also unmistakably confirms that the input of the claimed invention does not encompass functional specifications that include register-transfer level descriptions. (Ex. 4, November 1989 Amendment at 6-7) (emphasis added):

> [T]he **present invention distinguishes fundamentally over the prior art** by providing a system and **method for designing** an application specific integrated circuit at an **architecture independent** functional behavioral level. Thus, it is **not necessary for the user to have the specialized expert knowledge of a highly skilled VLSI design engineer**.
>
> * * *
>
> [I]t is clear from a complete reading of the patent specification in context that the specifications used by **Darringer et al. are not truly at an architecture independent level**, but rather are at a lower level which is indeed hardware architecture dependent and **defines the system at a "register-transfer" level description**. This is quite clear from the description at column 5 beginning at line 27.

Thus, this amendment demonstrates that specifications that include "register-transfer" level descriptions are not "architecture independent" and therefore, are not encompassed by the '432 patent's claimed invention. (*Id.*). Darringer et al. at 5:27-35 (Ex. 5) defines register-transfer level descriptions as a description that defines any control needed for the ASIC and consists of: 1) defining the inputs, outputs, and any registers of the proposed ASIC; and, 2) describing for a single clock cycle of the ASIC how the ASIC outputs and any registers are set according to the values of the ASIC inputs and the previous values of the registers.

As demonstrated above, one of ordinary skill in the art would understand that the '432 patent's file history unmistakably limits the '432 patent's claimed invention in three critical ways. First, the file history limits the claimed invention's input by excluding functional specifications having register-transfer level descriptions. Second, the input of the claimed invention is also limited to a flowchart format. Finally, the file history unambiguously requires that in translating the flowchart to a netlist, the step of selecting the hardware cells must be performed by a rule-based

expert system having an inference engine for applying the cell selection rules stored in the knowledge base of that rule-based expert system.

V. SYNOPSYS' POSITIONS ON THE PROPER CONSTRUCTION OF THE DISPUTED CLAIM TERMS IN THE '432 PATENT

In the following sections the proper meaning of the disputed claim terms of claims 13-17 will be discussed in the following manner. First the proper meanings for the disputed claim terms in claim 13 will be addressed and then the proper meanings for the disputed claim terms for claims 14-17 will be addressed. In addressing the proper meaning of claim terms for claim 13, all of the limitations are discussed, however, for clarity of explanation relating to the claimed method, the claim limitations have been loosely grouped as follows: preamble terms, input related issues, hardware cell selection using a rule-based expert system related issues, and the remaining limitations of the claim.

A. The Proper Construction of "A Computer-Aided Design Process For Designing"

The dispute regarding this claim limitation concerns Ricoh's inclusion of the phrase "during manufacture of a desired application specific integrated circuit (ASIC) chip that is designed to perform a specific purpose" and Synopsys' and Defendants' use of the phrase "as distinguished from a computer-aided manufacturing process, which uses a computer to direct and control the manufacturing process" in their respective proposed constructions. This dispute centers on Ricoh's effort to manufacture an argument that the "computer-aided design processes for designing application specific integrated circuits" somehow constitute processes "that are directly used in the manufacture of ASICs" pursuant to 35 U.S.C. § 271(g). Because Ricoh's proposal is contrary to the '432 patent's public record and Synopsys' and Defendants' proposal properly highlights the distinction between computer-aided design and computer-aided manufacturing as understood by persons of skill in the art from the '432 patent's public record, Ricoh's litigation induced attempt to alter the public record should be rejected.

First, the language in this limitation plainly provides that the claimed processes for claims 13-17 are "computer-aided design process for designing." (Ex. 1 at 16:34). The language is unambiguous to a person of skill in the art and does not support the inclusion of a computer-aided

manufacturing process. There is also nothing in the remaining claim limitations for claims 13-17 that supports broadening the claim to include anything other than design. In fact, the other limitations in the claims demonstrate that the claimed processes solely produce information or data representing the design of the desired ASIC. (Ex. 1 at 16:60-68) ("netlist" and "mask data").

Second, the '432 patent's description also states plainly that the invention "relates to the design of integrated circuits, and more particularly relates to a computer-aided method…for designing integrated circuits." (Ex. 1 at 1:9-12). This is consistent with the '432 patent's title: "Knowledge Based Method And Apparatus For **Designing** Integrated Circuits Using Functional Specifications." (Ex. 1) (emphasis added). Thus, like the claims, the '432 patent specification also demonstrates that the processes of claims 13-17 only produce information representing the design for the desired ASIC, *i.e.*, netlists and mask data. (Ex. 1 at 4:35-46).

Not only is Ricoh's proposed construction contrary to the '432 patent's claims and its specification, but it is also inconsistent with the statements made in the '432 patent's file history. Specifically, the April 1989 Amendment provides: "The present invention is a computer-aided design…method whereby the user can design application specific integrated circuits…." (Ex. 4, April 1989 Amendment at 8). Nothing in the '432 patent's file history supports Ricoh's attempt to broaden the claims to include a manufacturing process for a desired application specific integrated circuit (ASIC) chip.

Last, Ricoh's proposal seeks to distort the obvious distinction between "manufacturing" and "designing" an ASIC as understood by persons of ordinary skill in the art from the '432 patent's public record. Specifically, persons of skill in the art recognize that the processes for designing ASICs and the processes for manufacturing ASICs are separate, complex, and distinct sets of processes and that the processes for designing ASICs are simply **not** part of any of the processes for manufacturing ASICs. (Kowalski Decl. ¶¶ 7-10, 16-18, 65-66; *see also*, Ex. 7 at 7-24; Ex. 8 at 76-82 and 274-278).

In fact, the processes for design and the processes for manufacturing are separated by a third distinct and often-proprietary set of complex and expensive processes for manufacturing the photomasks (also known as masks) used in the manufacturing processes. (*Id.* ¶¶ 9, 18). Because of

the prohibitive cost of manufacturing these photomasks more than once for an ASIC chip, the goal of the designer is to perform these design processes only once. (*Id.* ¶ 18). Once the design is completed and the photomasks are made, the design processes (such as those in the '432 patent) are not performed again absent a desire or need to change the ASIC's design. This is vastly different from the ASIC manufacturing processes that must be performed each time the ASIC chips are made. *Id.*

Ricoh relies on statements that the "netlist" and/or "mask data" are "required" or "needed" "to produce the particular application specific integrated circuit in chip form" as support for its construction. (*See e.g.*, Ex. 1 at 2:44-49). But that does not mean that the '432 patent's "design" processes for generating design "data" are themselves part of the manufacturing process of the actual ASIC chips. A chip must be designed before it is manufactured and thereby produced.[7] However, this does not support Ricoh's attempt to blur the distinction between the manufacturing processes and the design processes for designing an ASIC. Design processes, like those claimed by claims 13-17, are simply not processes that are used to directly manufacture ASICs. In fact, in another article, the '432 patent's inventor recognizes that "design" processes and "manufacturing" processes are separate and distinct. (Ex. 9 at 364-365). Ricoh's proposal directly conflicts with the understanding of this claim limitation by persons skilled in the art.

B. **The Proper Construction of "Application Specific Integrated Circuit (ASIC)"**

The '432 patent explicitly defines this phrase as follows: "An application specific integrated circuit (ASIC) is an integrated circuit chip designed to perform a specific function, as distinguished from standard, general purpose integrated circuits, such as microprocessors, memory chips, etc." (Ex. 1 at 1:13-17). Defendants and Synopsys added the definition of "integrated circuit" for clarity.[8]

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[7] All of the statements relied on by Ricoh are consistent with the understanding of persons of skill in the art that "mask data" is used to manufacture the photomasks (also known as masks) that are in turn subsequently used in the other distinct and separate processes that are directly used in the actual manufacture of the ASIC chips. (Kowalski Decl. ¶ 8-9, 65-66).

[8] Ricoh's states (at page 13, footnote 9) that it does not oppose keeping the phrase "as distinguished from standard, general purpose integrated circuits, such s microprocessors, memory chips, etc." Yet, Ricoh still seeks to eliminate the phrase "as distinguished from standard, general purpose integrated circuits, such as microprocessors, memory chips, etc." from the definition of ASIC. Ricoh's attempt to exclude this "explicit" language from the '432 patent's definition of ASIC simply because it deems it to be "implicit" in its proposed definition is contrary to the '432 patent and should be rejected.

Synopsys' and Defendants' proposal for this disputed claim phrase, unlike Ricoh's proposal, incorporates the '432 patent's entire explicit definition for ASIC and comports with the meaning that one of skill in the art would assign to this phrase. (Ex. 1 at 1:13-17; Kowalski Decl. ¶ 19). The Court should, therefore, adopt Synopsys' and Defendants' proposed construction for "application specific integrated circuit."

C. The Claim Limitations Directed To The Input Of The Claimed Method For Claims 13-17

The following three claim limitations are directed to the input for the claimed processes of claims 13-17 for the '432 patent:

1. storing a set of definitions of architecture independent actions and conditions;
2. describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions;
3. specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed.

These three claim limitations should be construed consistently and as provided in portions C, D, E, K, L, and M in Synopsys' column of the Joint Claim Construction Chart. Specifically, these three claim limitations limit the input steps for the claimed method of claims 13-17 by requiring that:

1. the designer represents a sequence of logical steps and decisions in a flowchart format;
2. the designer assigns one stored definition for each logical step and decision described in the flowchart;
3. the flowchart input specification excludes a register transfer level (RTL) description, which defines any control at the clock cycle level needed for the ASIC.

Ricoh proposes constructions for these three claim limitations that attempt to alter the indisputable public record for the '432 patent and recapture claim scope that was relinquished to obtain allowance of claims 13-17. As demonstrated below, these three requirements are not only dictated by the public record for the '432 patent but are also consistent with the ordinary meaning of the claim language and the extrinsic evidence including expert testimony.

1. The Designer Represents A Sequence Of Logical Steps And Decisions In A Flowchart Format

The "describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions" claim language dictates that the "describing" be of "a series of

actions and conditions." Specifically, the prepositional phrase "for a proposed application specific integrated circuit" refers only to the fact that this "describing" step is performed for the proposed ASIC. The dispute here is focused on what is required by the language "describing . . . a series of architecture independent actions and conditions" in this step.

The '432 patent's specification defines the "describing . . . a series of architecture independent actions and conditions" step in claim 13 to require that "the designer represents a sequence of logical steps and decisions in a flowchart format." (Ex. 1 at Figs. 1a, 5, & 7; 2:21-27; 3:20-22; 3:50-59; 4:5-22; 4:35-38; 7:12-23). There is no question that the goal of the '432 patent is to make it possible for technicians not having VLSI design expertise to design ASICs. (Ex. 1 at 1:17-19; 2:14-20). The '432 patent plainly provides that this is achieved by allowing non-expert designers to define the input specifications for the proposed ASIC by representing a sequence of logical steps and decisions in a flowchart format. (Ex. 1 at 2:21-27, 4:11-18, 4:29-34). Not only is the ability to work with and define the input for the desired ASIC essential to achieve the '432 patent's goals but the flowchart editor software program is the only user interface described in the '432 patent. (Ex. 1). Moreover, despite Ricoh's claim to the contrary, the off-hand mention in the '432 patent to a "list format" without any explanation or any other description in the '432 patent as well as the use of the words "preferred" or "preferably" in describing the one and only flowchart input form embodiment in the '432 patent are simply not enough to support a broader interpretation for this step. *See e.g.*, *Biogen*, 318 F.3d at 1140 (Claims do not "'enlarge what is patented beyond what the inventor has described as [his] invention.'") (quoting *Network*, 242 F.3d at 1352); *Wang Labs.*, 197 F.3d at 1383 ("The usage 'preferred' does not of itself broaden the claims beyond their support in the specification.").

To the extent that there is any doubt that the '432 patent's specification requires that "the designer represents a sequence of logical steps and decisions in a flowchart format," such doubt is obliterated by the '432 patent's file history. Specifically, the file history unmistakably demonstrates the input of the claimed invention is limited to the designer's use of a flowchart editor to represent a sequence of logical steps and decisions in a flowchart format. (Ex. 4, April 1989 Amendment at 11; October 1989 Examiner Interview Summary; November 1989 Amendment at 7). The flowchart editor allows the designer to represent a sequence of operations in a flowchart having boxes

representing actions, diamonds representing conditions, and lines with arrows representing the transitions between those actions and conditions. (Ex. 4, Original Application at 13:1-11).

Like the specification, the file history also claims that the ability of non-expert designers to work with and define the input of the claimed invention is what distinguishes the '432 patent's invention over the prior art. (*See e.g.*, Ex. 4, April 1989 Amendment at 8). Time after time in the file history, the '432 patent's input specification was distinguished over the input specifications of the prior art cited during the file history because those inputs required the designer to posses specialized expert knowledge. (Ex. 4, April 1989 amendment at 9, 11-14, 16, 17, November 1989 amendment at 7). Thus, like the specification, the file history stresses the importance of enabling non-expert designers to design ASICs by allowing them to work with simple flowchart inputs to represent only the necessary logical steps.

Besides being dictated by the public record—*i.e.*, the '432 patent, its file history, and the cited prior art—the requirement that "the designer represents a sequence of logical steps and decisions in a flowchart format" is also supported by the dictionary definitions for the words describe, series, sequence, and operation. (Ex. 10 at 479; Ex. 11 at 343, 1073, 1074). These definitions are consistent with a requirement that the sequence of operations be represented in a flowchart format. (*Id.*).

Despite the overwhelming evidence in the '432 patent's public record, Ricoh proposes a construction that fails to acknowledge that the input specification of the '432 patent's claimed invention (including claims 13-17) is limited to a flowchart format. To support its position that the input specifications are not limited to a flowchart format Ricoh argues that: (1) the Examiner Interview Summary reflected only the examiner's beliefs and cannot be deemed an agreement reached between the examiner and applicant limiting the claims to a flowchart format; (2) that unlike some of the other claims, claims 13-17 were not amended and did not explicitly include the flowchart format feature of those other claims; and (3) requiring that the input specification be in a flowchart format would improperly exclude the so-called "list form" embodiment. Ricoh's arguments are neither supported by the intrinsic evidence nor the legal principles for claim construction.

First, contrary to Ricoh's claim, the Examiner Interview Summary explicitly states that the examiner and the applicant reached agreement. Specifically, the Examiner Interview Summary form

shows that the examiner checked the box providing: "**Agreement was reached** with respect to some or all of the **claims** in question." (Ex. 4 at October 1989 Interview Summary). After identifying all the claims discussed (which included claim 13 (application claim 20)), this Summary Form then provides the following lead-in to the examiner's summary. (Id.). ("Description of the general nature of **what was agreed to** if an agreement was reached, or any other comments:"). The actual summary then provides: "It is **agreed** that the features '**flowchart editor'** and 'expert system for translating the **flowchart** into a netlist defining the necessary hardware cells of the integrated circuit' are patentable [*sic*] distinct from the reference identified above." (*Id.*). The Examiner Interview Summary, read objectively, establishes that agreement was reached and that the features "**flowchart editor**" and "expert system for translating the **flowchart** into a netlist" were the examiner's only basis for allowing all of the claims including claim 13. *See, Biogen*, 318 F.3d at 1139 (district court correctly limited the claims based on objective reading of examiner's statements).

Equally misguided is Ricoh's argument that "[i]f the patentee intended to limit the patent claim 13 to the same scope (*i.e.*, flowchart format), the patentee would have used the same language, or at least added the term "flowchart" to patent claim 13, as patentee had done for patent claim 18." The Federal Circuit has flatly rejected this same argument. *See e.g., Biogen*, 318 F.3d at 1139; *ACCO Brands*, 346 F.3d at 1079 ("'It is incorrect to construe a claim as encompassing the scope that was relinquished in order to obtain allowance of another claim, despite a difference in words used.'") (emphasis added). Thus, neither Ricoh's failure to amend claim 13, nor the fact that claim 13 does not use the word "flowchart" change the unmistakable disclaimer in the '432 patent's file history relinquishing all formats other than the flowchart format.

Ricoh's argument that limiting claims 13-17 to a flowchart format improperly excludes so-called "list form" embodiment again ignores the intrinsic evidence as well as the Federal Circuit's precedent on claim construction. First, there is no "list form" preferred embodiment described in the '432 patent. *See* Section II.c. Moreover, the mere mention of a this "list form" cannot expand the claims beyond what is described and therefore, supported by the '432 patent's description. *See Wang Labs.*, 197 F.3d at 1383; *Bell Atl. Network*, 262 F.3d at 1273; *See also, Biogen*, 318 F.3d at 1140 (Claims do not "enlarge what is patented beyond what the inventor has described as [his] invention.")

(quoting *Network*, 242 F.3d at 1352). Besides, even assuming that there were a "list form" input specification embodiment described in the '432 patent (which there is not), here the unmistakable disclaimer in the '432 patent's file history of any input specification formats other than the flowchart format mandates excluding the disclaimed embodiment, even if it is a preferred embodiment. *See Springs Window Fashions*, 323 F.3d at 996; *Rheox, Inc.*, 276 F.3d at 1327 (disclaimer in file history is highly persuasive evidence warranting exclusion of preferred embodiment). Thus, Ricoh's arguments do not change the fact that the claimed invention of the '432 patent's input specifications is properly limited to a flowchart format.[9]

Finally, aside from its failure to acknowledge the requirement that the input specification must be in a flowchart format, Ricoh's proposed construction is also contrary to the claim language because it eliminates the requirement that the designer must describe "a series." Instead, Ricoh's proposal merely requires an input specification "containing the desired functions." Not only does this contradict the actual words used in the claim (*i.e.*, "describing…a series") but it is also contrary to the requirement in the patent's description that the designer must "describ[e] a sequence of logical operations." (Ex. 1 at 2:24-27). Last, Ricoh's construction would render the claimed method of claims 13-17 inoperative because without an input specification "describing the sequence" of the necessary logical steps and decisions to complete the ASIC's task, the necessary controller for synchronizing the operation of the other hardware cells could not be generated. (Kowalski Decl. ¶ 49). Thus, the Court should reject Ricoh's proposed construction and instead adopt Synopsys' and Defendants' proposal.

2. The Designer Assigns One Stored Definition For Each Logical Step And Decisions Described In The Flowchart

The "specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed" claim language

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[9] In fact, this requirement is also consistent with the inventor's own contemporaneous article, which claims that the flowchart input form is vital to system design and clearly distinguishes his invention from the prior art on this basis. (Ex. 2 at 379, 389).

requires that the "specifying" be of "one of said stored definitions which corresponds to the desired action or condition to be performed." Specifically, the prepositional phrase "for each described action and condition of the series" refers only to the fact that this "specifying" step is performed for each action and condition in the described series resulting from the previous "describing" step. Thus, the claim language for this "specifying" step requires that "the designer assigns one stored definition for each logical step and decision described in the flowchart."

Not only is this requirement mandated by the claim language but it is also apparent from the other '432 patent claims. Specifically, these other claims demonstrate that for each action and condition (operations) described, this step requires the designer to "specify" one stored definition (macro from a macro library) and that this "specifying" step and the previous "describing" step together are the steps that define the input specification for the claimed invention's method. (Ex. 1, claim 1 at 14:41-46, claim 9 at 15:39-45, claim 11 at 16:9-17). These other claims show that the functional input specifications of the '432 patent's claimed invention are defined by the designer in two separate steps: the first is the "describing" of the sequence of operations for the proposed ASIC in a flowchart and the second is the designer's "specifying" of one stored definition for each of those described operations in the flowchart. (*Id*.)

Besides being required by the language of the '432 patent's claims, the requirement that "the designer assigns one stored definition for each logical step and decision described in the flowchart" is also supported by the specification. Specifically, the '432 patent also demonstrates that this "specifying" step and the previous "describing" step together are the steps that define the input specification for the claimed invention's method and that the "specifying" step requires the designer to assign one stored definition (macro) for each logical step and decision (operation) described in the flowchart. (Ex. 1 at 5:20-22; 7:24-26; 8:51-55); (*See also*, Ex. 1 at Fig. 5, 3:20-22; 4:61-63; 8:23-26) Finally, the requirement that the "designer" does the "assigning" of the stored definitions is also consistent with the dictionary definition for "specify." (Ex. 11 at 1132) (Specify – to name or state explicitly or in detail; to include as an item in a specification). These definitions imply that "specifying" is an act performed by a person.

Ricoh's proposed construction is contrary to the actual words used in the claim. First, the claim language unambiguously requires that this "specifying" step be performed "for each described action and condition of the series." Ricoh's proposal improperly seeks to eliminate this explicit connection between the "describing" and the "specifying" steps by replacing the phrase "for each described action and condition of the series" with the phrase "for each desired function to be performed by the desired ASIC." Ricoh's attempt to broaden this unambiguous claim language is simply not supported by the '432 patent's public record and is in fact contrary to it.

Ricoh also wrongly claims that the term "specifying" is redefined by the '432 patent's specification to mean "mapping or associating a desired function to be performed by the manufactured ASIC with a definition from the library of definitions." Ricoh attempts to support this extraordinary redefinition of the word "specifying" by: (1) quoting to portions of the '432 patent that actually support Synopsys' and Defendants' proposed construction (*See e.g.*, Ex. 1 at 7:24-25); and (2) claiming that this redefinition is necessary to avoid excluding yet another so-called embodiment in the '432 patent.

First, the '432 patent demonstrates that this "specifying" refers to the designer assigning one stored definition for each described action and condition in the series of the previous "describing" step. (Ex. 1 at 7:24-26; 8:51-56). Thus, "specifying," consistent with its ordinary dictionary meaning and description in the '432 patent's specification refers to the "designer's assigning" and not to any automated "mapping or associating" as Ricoh claims. Second, contrary to Ricoh's claim, there is no embodiment described in the '432 patent for "automatically mapping" each described action and condition in the series with the stored definitions for those actions and conditions. *See* Section II. d.[10] Besides, even if there were an automatic mapping embodiment (which there is not), the existence of such an alternative embodiment, by itself, would not support the extraordinary redefinition of "specifying" proposed by Ricoh.

[10] Equally misguided is Ricoh's argument that Synopsys' and Defendants' construction for this step is "particularly improper" because it excludes this nonexistent embodiment.

3. The Flowchart Input Specification Excludes A Register Transfer Level (RTL) Description, Which Defines Any Control Needed For The ASIC At The Clock Cycle Level

This dispute centers on the effect of Ricoh's adding the completely new phrase "architecture independent" throughout the patent application in an attempt to distinguish the claimed invention over the prior art, including Darringer et al. (Ex. 4, April 1989 Amendment at 1-8). Specifically, the phrase "architecture independent" was added to the claims, and the specification including the Summary of the Invention, and the Abstract of the Disclosure. (*Id.*).[11]

Ricoh added this vague phrase to argue before the United States Patent Office that the phrase "architecture independent" distinguished the claimed invention over prior art functional specifications because they include register-transfer level descriptions. Now, however, standing before this Court, Ricoh wishes to take the diametrically opposed position, *i.e.*, that register-transfer level descriptions are not excluded by the phrase architecture independent. This is a classic example of ignoring the public record and treating the claims as a nose of wax.

The original application for the '432 patent was directed towards the input of functional specifications, which were comprised of a series of actions and conditions. (Ex. 4, Original Application at 1, 3, 4-5, 6, 7, 8, 29, 30, and 34). The original application for the '432 patent and the issued '432 patent demonstrate that the "series of actions and conditions" are the "sequence of logical operations" necessary to complete the task of the ASIC to be designed and that those logical operations consist of actions (steps) and conditions (decisions). (Ex. 1 at 2:24-27; 3:20-22; 3:52-55; 6:1-54; Ex. 4, Original Application at 5:12-13; 6:11-13; 10:21-12:9). The question here is: how did Ricoh's adding of the phrase "architecture independent" alter the meaning of the "series of actions

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[11] The phrase "architecture independent" is vague and imprecise. (Kowalski Decl. ¶ 22). It is also not defined in the '432 patent. (Ex. 1). Because this phrase is used in claims 13-17, therefore, it renders them all invalid for failing to meet the "definiteness" requirement of 35 U.S.C. § 112. U.S.C. § 112 ¶ 2. ("The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention."). In addition to being invalid pursuant to § 112, claims 13-17 are also invalid because the addition of "architecture independent" to the claims and specification constituted "new matter," which is prohibited by 35 U.S.C. § 132. 35 U.S.C. § 132(a). ("No amendment shall introduce new matter into the disclosure of the invention.").

and conditions" that comprise the input functional specifications of the claimed invention? The file history provides the answer to that question.

The prior art described functional input specifications. (*See e.g.*, Ex. 5 at 5:21-26; 14:61-63). The applicant admitted this fact during the file history. (Ex. 4, April 1989 Amendment at 9). Because of this, the patent examiner properly rejected all of the claims. (Ex. 4, January 1989 rejection at 1-3). More than a year after the original application was filed, the applicant added the phrase "architecture independent" to distinguish the cited prior art. (Ex. 4, April 1989 amendment at 1-10).

At the same time that the applicant added the phrase "architecture independent" to the specification and all of the claims, the applicant repeatedly argued that the input specifications of the prior art including Darringer et al. were not "architecture independent" simply because their input specifications included register-transfer level descriptions. (Ex. 4, April 1989 Amendment at 9 and 12-13, November 1989 Amendment at 7). Because of this amendment and the arguments made by the applicant in the '432 patent's file history, the applicants addition of "architecture independent" to the claims excluded register-transfer level descriptions from the claimed invention. (Ex. 4, April 1989 amendment at 9 and 2-13, November 1989 amendment at 7). In other words, the applicant argued that the claimed invention was different from the prior art because it excluded register-transfer level descriptions (*See e.g.*, Ex. 4, April 1989 Amendment at 9). The file history, therefore, unmistakably demonstrates that "architecture independent" excludes register-transfer level descriptions and that anything including register-transfer level descriptions cannot be encompassed by the claimed invention. *See Springs Window Fashions*, 323 F3d at 995-96. This is again consistent with the inventor's own contemporaneous article, which provides that the input of his invention "is not an RT-level description." (Ex. 2 at 388).

The file history and the Darringer et al. prior art also show that register-transfer level descriptions are descriptions that define any control needed for the ASIC at the clock cycle level, which consists of: 1) defining the inputs, outputs, and any registers of the proposed ASIC; and, 2) describing for a single clock cycle of the ASIC how the ASIC outputs and any registers are set according to the values of the ASIC inputs and the previous values of the registers. (Ex. 5 at 5:27-

35); *See Kumar*, 351 F.3d at 1368 (adopting definition of term in cited prior art which is intrinsic evidence).

Ricoh proposes a definition for "architecture independent actions and conditions" that would include any "functional or behavioral aspects of a circuit (or circuit segment) that does not imply any set architecture, structure, or implementing technology." Ricoh's definition improperly ignores the fact that the phrase "architecture independent" was not in the original application and was added along with repeated arguments that adding the phrase "architecture independent" limited the functional specifications (comprised of a series of actions and conditions) by excluding register-transfer level descriptions that were included in the prior art functional specifications.

First, Ricoh attempts to mask the fact that its definition of "architecture independent" was formed through the improper use of a general-usage dictionary's definitions for the terms "architecture" and "independent" by taking issue with Synopsys' and Defendants' defining "architecture independent" and "actions and conditions" separately. Synopsys' and Defendants' definition, which takes into account the affect of adding the completely new phrase "architecture independent" to the claims and the specification in light of the '432 patent's file history is certainly proper and mandated by Federal Circuit authority. In contrast, Ricoh's attempt to define the technical phrase "architecture independent" with a general-usage dictionary is improper and should be rejected. *See Vanderlande*, 366 F.3d at 1321 (where one of skill in the art would attach no meaning at all to claim term general-usage dictionaries are irrelevant).

Second, Ricoh incorrectly claims that its definition "can be ascertained from the '432 patent." To support this conclusion, Ricoh relies on FIG. 1a and portions of the specification, which were also amended to include the phrase "architecture independent." (Ex. 1 at 2:6-14; 3:50-57). These portions of the '432 patent support Synopsys' and Defendants' proposal for "actions and conditions," *i.e.*, "the logical steps and decisions that are represented as rectangles and diamonds in the flowchart." Because the specification and the claims were both amended to add the phrase "architecture independent," these portions of the patent do not provide any guidance on the difference between "architecture independent actions and conditions" of the amended '432 patent application and the "actions and conditions" of the original '432 patent application. Thus, Ricoh's definition of

the technical phrase "architecture independent," which is improperly formed from the general-usage dictionary definitions of the words "architecture" and "independent," should be rejected.

Next, Ricoh misleadingly claims that Synopsys' and Defendants' claim construction proposal, which gives effect to the unmistakable disclaimer of subject matter in the file history, is an improper non-infringement argument. Ricoh is wrong. Synopsys' and Defendants' proposal properly relies on the indisputable public record to show that Ricoh disclaimed the "register-transfer" level descriptions described in the Darringer prior art from the scope of its claimed invention. *See e.g., Southwall*, 54 F.3d at 1576.

In fact, it is Ricoh that makes infringement arguments in its opening brief. Specifically, Ricoh, recognizing that its repeated arguments to the patent office disclaimed functional specifications that included register-transfer level descriptions from the scope of the claimed invention, argues now that the Court should "clarify" that only "basic" or "primitive RTL" was disclaimed from the scope of the claimed invention and not "functional RTL." Not surprisingly, Ricoh then characterizes the Verilog and VHDL hardware description languages ("HDLs") it accuses of infringement as examples of "functional" register-transfer level languages. This directly contradicts the '432 patent's file history where Ricoh repeatedly distinguished the prior art HDLs, which Ricoh claimed required the VLSI design expertise that is not required for using the method of the claimed invention. (Ex. 4, April 1989 Amendment at 9, 11, 13, 15 and 17; *see e.g.*, Ex. 12 at 3, 7; Ex. 13 at 73-74). Ricoh's made up distinction is not only contrary to the file history but it also finds no support in the other parts of the '432 patent's public record or anywhere else.

In fact, the '432 patent's public record fails to provide any support for Ricoh's conjured up distinction between "basic" or "primitive RTL" and "functional RTL." The '432 patent's public record never mentions the terms "basic RTL," "primitive RTL," or "functional RTL." Ricoh attempts to support its distinction by simply mischaracterizing the Darringer prior art patent. Specifically, Ricoh claims that the Darringer prior art patent describes a "'basic' or 'primitive Boolean'-type" of register-transfer level description simply because the register transfer-level description can be translated into AND/OR (*i.e.*, Boolean) logic. Ricoh is wrong.

The Darringer prior art patent specifically defines a register-transfer level description and the subsequent translation or transformation steps described in that patent do not alter this explicit definition. (Ex. 5, 5:27-35). Given this and the fact that the '432 patent file history explicitly disclaims all register-transfer level descriptions without a single reference to any so-called "basic," "primitive," or "functional" "types" of RTL, Ricoh's completely unsupported attempt to limit the unmistakable disclaimer of register-transfer level descriptions should be rejected out-of-hand.

Last, Ricoh again mischaracterizes the '432 patent's description in yet another attempt to claim that Synopsys' and Defendants' proposed construction excludes a preferred embodiment. Specifically, Ricoh claims that the example functional specification shown in FIG. 10 mandates a narrowing of the prosecution history disclaimer. FIG. 10 merely shows a sequence of actions and conditions with specified macros but without any register-transfer level description. Ricoh does not point to anything in FIG. 10 that meets the Darringer patent's definition of a register-transfer description. Besides its failure to support this argument, even if an interpretation excluded an example described in the patent (which is not the case here), Ricoh's unmistakable disclaimer in the '432 patent's file history of any input functional specifications that include a register-transfer level description warrants excluding even a preferred embodiment. *See Springs Window Fashions*, 323 F3d at 996; *Rheox, Inc.*, 276 F.3d at 1327.

D. **The Proper Construction of "Data Describing A Set Of…Hardware Cells…"**

This claim limitation "storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set" should be construed consistently and as provided in portions F and G in Synopsys' column of the Joint Claim Construction Chart. Specifically, this claim limitation limits the claimed invention of claims 13-17 by requiring that: 1) there be at least one hardware cell for each stored definition; and, 2) each named hardware cell has corresponding descriptions at the functional level, logic level, circuit level, and layout level that are all defined.

Claim 13 and the '432 patent specification requires that there be at least one hardware description for each of the stored definitions (macros in the macro library). (Ex. 1 at FIG. 4; 5:22-25) ("For each macro function in the macro library 23 there may be several hardware cells in the cell

library 34 . . . "). Because it is necessary to match a hardware cell description for each stored definition specified in the flowchart, there must be at least one hardware cell description for each stored definition that can be specified. (Ex. 1 at 8:31-33). Thus, the ability to design ASICs depends on the fact that there is at least one hardware description for each of the stored definitions. (*Id.*).

Not only is this requirement supported by the '432 patent but the claimed method for claims 13-17 would be inoperative if there were not at least one corresponding hardware cell description to match to the stored definitions that have been specified in the flowchart. Therefore, there must be at least one hardware description for each of the stored definitions that can be specified in the flowchart. Otherwise, accepting Ricoh's position, the method would not be able to generate a netlist if one of the specified stored definitions was a stored definition without any corresponding hardware description to which it could be mapped. Despite this, Ricoh simply argues, without any explanation, that there is no support for this requirement. The Court should adopt Synopsys' and Defendants' proposal.

Claim 13 and the '432 patent specification also require that each named hardware cell have corresponding descriptions at the functional level, logic level, circuit level, and layout level that are all defined. (Ex. 1 at Fig. 4; 2:34-39; 3:59-67; 5:15-20; 5:23-25; 9:24-51). Specifically, the specification defines the "data describing" the hardware cells as descriptions at the functional level, logic level, circuit level, and layout level. (Ex. 1 at 9:24-34). Additionally, such information is essential for matching the specified stored definitions to these hardware cell descriptions and for producing the netlist and mask data for the ASIC. (Ex. 1 at 5:15-20; 8:60-64). Simply stated, without these functional, logic, circuit, and layout level definitions for each hardware cell, the ASIC could not be designed using the '432 patent's claimed invention. (*Id.*).

While Ricoh disputes that each hardware cell description must have defined descriptions at the functional level, logic level, circuit level, and layout level, Ricoh, at the same time, admits that the hardware cells are defined to "have specific physical and functional characteristics used as building blocks for implementing an ASIC to be manufactured." In order for the hardware cells to be defined by "specific physical and functional characteristics" of "previously designed hardware cells" as Ricoh admits is necessary, the "data describing" must have corresponding descriptions at the functional level, logic level, circuit level, and layout level that are all defined. Thus, Ricoh's own

proposal for the definition of hardware cells supports Synopsys' and Defendants' proposed construction.

E. The Claim Limitations Directed To Selecting Hardware Cells Using A Rule-Based Expert System

The following two claim limitations are directed to the step of selecting hardware cells using a rule-based expert system for the claimed processes of claims 13-17 for the '432 patent:

1. storing in an expert system knowledge base a set of rules for selecting hardware cells to perform the actions and conditions;
2. selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit, said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base.

These two claim limitations should be construed consistently and as provided in portions H, I, J, N, and O in Synopsys' column of the Joint Claim Construction Chart. Specifically, these two claim limitations limit the claimed method of claims 13-17 by requiring that:

1. a rule-based expert system software maps each specified definition in the flowchart to a stored hardware cell description;
2. unlike conventional software, the rule-based expert system software uses an inference engine to selectively apply the rules stored in the knowledge base; and,
3. unlike conventional software, the rule-based expert system software uses a set of IF-THEN rules to map the specified definitions to the stored hardware cell descriptions.

Ricoh proposes constructions for the above two limitations without these three requirements. Ricoh does this in an attempt to alter the indisputable public record for the '432 patent and recapture claim scope that was relinquished to obtain allowance of claims 13-17. As demonstrated below, these three requirements are not only dictated by the public record for the '432 patent (*i.e.*, the claims, specification, and file history) but are also consistent with the ordinary meaning of the technical terms of art "expert system," "knowledge base," and "rules" as evidenced by contemporaneous technical dictionaries, texts, treatises, etc. from around the time the application for the '432 patent was filed.

1. Rule-Based Expert System Maps Each Specified Definition In The Flowchart To A Stored Hardware Cell Description

The language in claim 13 dictates that mapping the specified definitions to the stored hardware cell descriptions must be performed by a rule-based expert system and not conventional software. (Ex. 1 at 16: 42-44; 16:56-60) ("storing in an expert system knowledge base a set of rules for selecting hardware cells" and "said step of selecting a hardware cell comprising applying…a set of cell selection rules stored in said expert system knowledge base"). A person of ordinary skill in the art would understand this language as requiring the selecting step to be performed by a rule-based expert system. (Kowalski Decl. ¶ 56-57). To construe these limitations otherwise would constitute an improper redrafting of the claims that eliminates explicit requirements in the language used.

Besides being dictated by the claim language itself, the '432 patent's specification also mandates that a rule-based expert system be used to select the hardware cells. (Ex. 1 at Abstract; 2:58-63; 8:29-37; 8:58-60). For example, on the first page of the '432 patent, the Abstract states that the present invention's "method uses artificial intelligence and expert system technology…to select the…hardware cells." (*Id*. at Abstract). Even more compelling are the statements in the '432 patent's description that the "mapping needs the use of artificial intelligence techniques because the cell selection process is complicated" and that the "Cell Selector uses a rule based expert system to select the appropriate cell or cells to perform each action." (*Id*. at 8:58-60). Simply stated, the claim language and the '432 patent's specification both require that mapping the specified definitions to the stored hardware cell descriptions be performed by a rule-based expert system.

Such a requirement is not only evident from the claims and the specification, but any reasonable competitor reviewing the '432 patent's file history and the prior art distinguished in that file history would conclude that these two limitations require that a rule-based expert system software be used for mapping the specified definitions to the stored hardware cell descriptions. Specifically, this conclusion is inescapable for any person of skill in the art in view of the statements made regarding these limitations, the unambiguous arguments made when these limitation were added to

claim 13 (original application claim numbers 20, 21, and 25)[12], the examiner interview summary, and the prior art that was distinguished based on these limitations in the '432 patent's file history.

First, in the April 1989 Amendment in the '432 patent's file history, it was argued that using a rule-based expert system to select hardware cells distinguished the '432 patent's invention from the prior art. (Ex. 4, April 1989 Amendment at 10). In that same amendment, it was also argued that Darringer et al. did not teach the claimed method of application claim 21 because it "provides a knowledge base in the form of a **rule based** automatic logic synthesis component, *i.e.* an **expert system**." (*Id*. at 9) (emphasis added). This amendment demonstrates that mapping the specified definitions to the stored hardware cell descriptions must be performed by a rule-based expert system and not conventional algorithmic software that was known and disclosed in the prior art, including in Darringer et al.

Second, the summary of the October 1989 examiner interview and the November 1989 Amendment reveal that the limitations: 1) "storing in an expert system knowledge base a set of rules for selecting hardware cells to perform the actions and conditions;" and, 2) "said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base" were added to claim 13 (application claim 20) to claim the feature of an expert system for translating a flowchart to a netlist. That summary provides:

> It is **agreed** that the **features** "flowchart editor" and "**expert system for translating the flowchart into a netlist defining the necessary hardware cells of the integrated circuit**" are patentable [*sic*] distinct from the reference identified above. Thus, applicant's attorney **will** amend the claims to include **those features**.

(Ex. 4, Examiner Interview Summary) (emphasis added). In the November 1989 Amendment following this interview, claim 13 (application claim 20) was amended to add the step of "generating

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[12] Claim 13 of the issued '432 patent corresponds to application claim 20. Application claim 20 was amended during the file history to add the requirement of using a rule-based expert system by adding the limitation of application claim 21 to the selecting step. At the same time, the additional generating step of application claim 25 of the original patent application was also added to application claim 20.

for the selected integrated circuit hardware cells, a netlist…" from application claim 25 and the requirement from application claim 21 that the prior selecting step be performed by "applying…a set of cell selection rules stored in said expert system knowledge base." The limitation "storing in an expert system knowledge base a set of rules for selecting hardware cells …" was also added to claim 13 to provide the proper antecedent basis for the added phrase "cell selection rules stored in said expert system knowledge base." Thus, claim 13 was amended to distinguish over the Darringer et al. prior art reference by requiring the mapping of the specified definitions in the flowchart to the stored hardware cell descriptions to be performed by a rule-based expert system.

Ricoh claims that the term "expert system knowledge base" "is intended to capture the features of a 'knowledge base' that may be used in an expert system, but not intended to capture an "expert system" that uses a 'knowledge base.'" Ricoh's claim directly contradicts the '432 patent's public record. First, the April 1989 Amendment demonstrates that the addition of the language "applying . . . a set of cell selection rules stored in said expert system knowledge base" to application claim 20 (issued claim 13) from application claim 21 requires the use of a rule-based expert system for the mapping of the specified definitions to the stored hardware cell descriptions. (Ex. 4, April 1989 Amendment at 9-10). Second, when the limitation from application claim 21 was added to application claim 20 (issued claim 13), in the November 1989 Amendment, applicant explicitly stated that "Independent Claim 20 has also been amended to emphasize the expert system aspects of applicants' method." (*Id.*, November 1989 Amendment at 9). Last, the '432 patent and its file history, consistent with the extrinsic evidence, demonstrate that the terms "expert system knowledge base," "knowledge based expert system," "rule-based expert system," and "knowledge base" are all used synonymously to refer to an expert system having an inference engine and a knowledge base containing the rules embodying the expert knowledge as distinguished from conventional software programs. (Ex. 1 at 2:53-64; 5:25-29; 8:58-60; Ex. 4, April 1989 Amendment at 9; Kowalski Decl. ¶ 35; Ex. 14 at 140).

Equally misguided is Ricoh's attempt to broaden the requirement that "mapping the specified definitions to the stored hardware cell descriptions must be performed by a rule-based expert system" to its proposal, which is "selecting…a hardware cell for performing the desired function of the

desired ASIC through the application of the rules." Ricoh's proposal is contrary to the '432 patent's public record.

As demonstrated above, the language "applying . . . a set of cell selection rules stored in said expert system knowledge base" requires that the mapping be done by a rule-based expert system as defined more fully below. Ricoh's use of the phrase "through the application of the rules" attempts to eliminate the requirement from the file history that a rule-based expert system be used. Second, the language "selecting …for each of the specified definitions a corresponding integrated circuit hardware cell" requires "mapping each of the specified definitions to a stored hardware cell description." This is evident from the claim language and the '432 patent's description. (Ex. 1 at 6:28-31; 6:53-54; 8:58-60; 9:21-23; 9:51-61). Ricoh's attempt to eliminate the requirement that "each specified definition" be mapped to "a corresponding hardware cell" is contrary to the '432 patent's public record. For these reasons, Ricoh's attempt to broaden this "selecting step" contrary to the '432 patent's claims, specification, and its file history should be rejected.

2. Unlike Conventional Software, Rule-Based Expert System Software Uses An Inference Engine To Selectively Apply The Rules Stored In The Knowledge Base

This requirement deals with the critical and important distinction in the claims, the '432 patent specification and its file history between two different approaches for selecting hardware cells: 1) rule-based expert system software; and, 2) conventional algorithmic software. Specifically, the rule-based expert system software claimed in the patent for performing the mapping step must comprise an inference engine, a knowledge base, and a working memory, which enable the inference engine to selectively apply the rules stored in the knowledge base to what is stored in the working memory (as distinguished from conventional algorithmic software, which uses a predefined step-by-step procedure). A person of ordinary skill in the art in 1988 would have known that the rule-based expert system software approach is substantially different than using conventional algorithmic software. Indeed, this distinction is evident from the technical dictionaries, texts, and treatises existing at the time the application for the '432 patent was filed and confirmed by the inventor's own contemporaneous article.

An expert system is software that attempts to embody the knowledge of a human expert in a particular field and then use that knowledge to simulate the reasoning of such an expert to solve problems in that field. (Ex. 15 at 9-10, Ex. 14 at 86-87, Ex. 16 at 136). This particular type of software operates nothing like conventional software, which uses a predefined step-by-step procedure (or algorithm) for solving problems. (Ex. 6 at 1:30-54, Ex. 15 at 7-10; Ex. 14 at 6). Instead, expert systems use non-procedural processing to solve problems—*i.e.*, they solve problems through the application of the rules in the knowledge base. (Ex. 15 at 7-10).

An expert system is comprised of (i) a knowledge base containing the rules, written in IF-THEN format, which embody the expert knowledge in the particular field and (ii) an inference engine for selectively applying those rules. (Ex. 15 at 9-10, 74-75, and 99-110, Ex. 17 at 10-15, Ex. 14 at 86-87, 140, and 223, Ex. 18 at 8, Ex. 19 at 11-12, and Ex. 20 at 13-20). The rules have an antecedent portion (IF) and a consequent portion (THEN). (Ex. 15 at 74-75, Ex. 17 at 10-11, Ex. 18 at 8, Ex. 21 at 269, Ex. 20 at 14-15; Ex. 14 at 10, 53). The inference engine uses search and pattern matching techniques to selectively apply the rules in the knowledge base. (Ex. 15 at 10, Ex. 17 at 9-11). The application of these rules solves the particular problem in the field—not any predefined step-by-step procedure (*i.e.*, algorithm) as in conventional software.

Ignoring how persons of ordinary skill in the field of the invention understand expert systems technology, Ricoh proposes constructions for these two limitations that seek to alter the public record for the '432 patent by attempting to blur this critical distinction between rule-based expert system software and conventional algorithmic software so that it can later argue that claims 13-17 encompass the conventional algorithmic software that it unambiguously disclaimed to obtain these claims of the '432 patent.

First, as explained above, the language in claim 13 dictates that the mapping must be performed by a rule-based expert system and not conventional software. (Ex. 1 at 16: 42-44; 16:56-61). A person of skill in the art would understand this language to require that the selecting step uses one approach, *i.e.*, an expert system inference engine to apply a set of IF-THEN rules stored in the expert system knowledge base to the specified definitions stored in the working memory of the expert system as opposed to using the other approach, *i.e.*, conventional algorithmic software, which uses a

predefined step-by-step procedure. (Kowalski Decl. ¶ 56-57).

The distinctions between these two different approaches is also consistent with the inventor's (Dr. Kobayashi's) own 1989 article about the same KBSC system described in the '432 patent. (Ex. 2 at 351). That article confirms that to one skilled iin the art at the time of the filing, there were only two approaches and that the KBSC system was directed to using an inference engine to apply the IF-THEN rules contained in the knowledge base of a rule-based expert system and not the conventional algorithmic approach of the prior art. (*Id.* at 379-380 and 389).

The importance of the distinctions between the rule-based expert system approach and the conventional algorithmic software approach is also evident from the '432 patent's specification. For example, the specification provides that "mapping needs the use of artificial intelligence techniques because the cell selection process is complicated." (Ex. 1 at 8:34-37). This conveys to a person of ordinary skill in the art that the invention is directed to the use of rule-based expert system software and not conventional algorithmic software. (Kowalski Decl. ¶ 41, 44, 56-57). In fact, nothing in the '432 patent's specification even suggests to a person of skill in the art to use conventional algorithmic software instead of rule-based expert system software to select hardware cells.

Not only is the distinction between expert system and conventional software evident from the claims and the specification, but any reasonable competitor reviewing the '432 patent's file history and the prior art distinguished in that file history would conclude that the expert system software and conventional software are two distinct and substantially different approaches. (Ex. 4, January 1988 rejection, April 1989 amendment, August 1989 rejection, November 1989 amendment). Specifically, this is evident from the prior art that the applicant distinguished during the '432 patent's file history. (Ex. 4, April 1989 amendment at 9-10, 13, Interview Summary, and November 1989 amendment at 7-8); Ex. 6 at 1:30-56).

The '432 patent's file history also defines the "expert system knowledge base" as a knowledge base containing the rules and an inference engine for applying those rules. (Ex. 4, November 1989 Amendment at 2, 8). Given that the language "applying…a set of cell selection rules stored in said expert system knowledge base" was added to "emphasize the expert system aspects of applicants' method," the "expert system knowledge base" certainly requires "a knowledge base

containing rules for selecting hardware cells" and an "inference engine" for selectively applying those rules "for selecting appropriate hardware cells." (*Id*. at 2-3, 8-9). Thus, Ricoh's claim, in its brief, that nothing mandates that the "expert system knowledge base" have an "inference engine" not only ignores how persons in the field of the invention (including the '432 patent's inventor) would understand that term, but it is also contrary to the '432 patent's public record.

3. Unlike Conventional Software, The Rule-Based Expert System Software Uses A Set Of IF-THEN Rules For Mapping Specified Definitions To Stored Hardware Cell Descriptions

The '432 patent also unmistakably defines the "rules" used by the rule-based expert system of the claimed invention to be IF-THEN rules. (Ex. 1 at 11:1-15) (*see also* 11:48-12:30). This definition is consistent with the understanding of one of skill in the art as demonstrated by the relevant technical dictionaries, treatises, and the prior art. (Ex. 15 at 74-75, Ex. 17 at 10-11, Ex. 14 at 10, 53, Ex. 18 at 8, Ex. 21 at 269, Ex. 20 at 14-15).

The fact that the claimed invention of the '432 patent requires the use of "IF-THEN rules" is also demonstrated by the inventor's own contemporaneous article. (Ex. 2). That article described the same KBSC software described in the '432 patent and unequivocally asserts that IF-THEN rules were used by the KBSC software. (*Id* at 379, 381.). Thus, contrary to Ricoh's claims in its opening brief, persons of skill in the art (including the '432 patent's inventor) would understand the public record for the '432 patent to require that each rule have "an antecedent portion (IF) and a consequent portion (THEN)."

Aside from the fact that Ricoh's criticisms of Synopsys' and Defendants' proposal are unfounded, Ricoh improperly relies on a general-usage dictionary for its own definition of "rule" a technical term of art. Specifically, despite admitting that the "IF-THEN" rules are the only ones supported by the '432 patent's description, Ricoh, relying on a general-usage dictionary, proposes that these "rules" need only be "formulated as prescribed procedures." Ricoh's attempt to alter the definition of the technical term of art "rules" as understood by persons of skill in the art from the '432 patent to a definition from a general-usage dictionary is contrary to claim construction law. *See e.g.*, *Vanderlande*, 366 F.3d at 1321. Thus, the Court must define the "rules" to require both "an

antecedent portion (IF) and a consequent portion (THEN)" and Ricoh's attempt to broaden the '432 patent's disclosure to encompass "prescribed procedures" should be rejected.

The claim language "a set of rules for selecting hardware cells" and "said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base" requires that the IF-THEN rules stored in the knowledge base of the rule-based expert system embody the expert knowledge for mapping the specified definitions in the flowchart to the hardware cell descriptions. (Ex. 1 at 14:48-54). This is also demonstrated by the other claims in the '432 patent. (Ex. 1 at 14:57-59; 15:56-58; 18:6-8).

Aside from being dictated by the language in the claim 13 and the other claims, the '432 patent's specification also unmistakably requires that the IF-THEN rules stored in the knowledge base of the rule-based expert system embody the expert knowledge for mapping the specified definitions in the flowchart to the hardware cell descriptions. (Ex. 1 at 8:58-9:5). The "cell selection rules" referred to in this selecting step are the IF-THEN rules for "mapping macros to cells." (*Id.*). Thus, the "set of cell selection rules" are the set of IF-THEN rules of the rule-based expert system that embody the expert knowledge that is essential for mapping the specified definitions in the flowchart to the hardware cell descriptions.

Ricoh attempts to eliminate this claim requirement by proposing that the "rules" only "comprise the expert knowledge of highly skilled VLSI designers." The claim language and the '432 patent's description, however, requires that the rules not only embody the expert knowledge of highly skilled VLSI designers but that the "expert knowledge" be <u>for mapping the specified definitions in the flowchart to the hardware cell descriptions</u>. (Ex. 1 at 8:21-23; 8:34-37).

Last, Ricoh's definition for "rules" - "the expert knowledge of highly skilled VLSI designers formulated as prescribed procedures" - must be rejected because it would encompass the Darringer prior art patent, which was distinguished in the file history. (Ex. 4 at April 1989 Amendment at 9-10). Specifically, the Darringer prior art patent contains "the expert knowledge of highly skilled VLSI designers formulated as prescribed procedures" in the form of the procedures and transformations. (Ex. 5 at 7:32-9:35; Kowalski Decl. at ¶ 40). Thus, contrary to Ricoh's proposal,

"the set of rules" cannot be properly defined to encompass the procedures and transformations in the prior art because Ricoh disclaimed such a construction by arguing that Darringer had no knowledge base of any kind. *See e.g., Southwall,* 54 F.3d at 1576.

F. The Proper Construction of "Generating For The Selected Integrated Circuit Hardware Cells, A Netlist…"[13]

The claim language "generating **for the selected integrated hardware cells**, a netlist" is unambiguous. That language demonstrates that "generating . . . a netlist" step is a separate step that must come after the step of "selecting" hardware cells. This is also evident from the '432 patent's specification, which provides that the "netlist is generated **after** the cells have been selected . . . " (Ex. 1 at 9:64-65) (emphasis added).

Finally, the '432 patent's file history reveals that the generating step (application claim 25) is a separate step that follows the selecting step that was added to claim 13 (application claim 20) in an amendment where the applicant could not create "new issues." (Ex. 4, November 1989 Amendment at 6). That amendment incorporated the limitation from application claim 21 into claim 13 (application claim 20) and added the further generating step of application claim 25. (*Id.* at 4-5) The original claims 21 and 25 demonstrate that claim 21 limited the selecting step by adding a further limitation and claim 25 added the further generating step after that selecting step. (Ex. 4, Original Application at 35-36). For these reasons, Ricoh's attempt to broaden the claimed invention by incorporating this step into the previous selecting step based solely on the additional "; and" before the selecting step should be rejected.

1. This Generating Step Requires Eliminating Unnecessary Hardware Cells That Have Been Selected

The claim language "generating **for the selected…hardware cells**, a netlist defining the **hardware cells which are needed** to perform the desired function of the integrated circuit" requires

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[13] Like Ricoh's attempt to add the phrase "During manufacture…" to the construction of "computer-aided design for designing," Ricoh's attempt to add the phrase "the netlist is passed to the next subsequent step in the process for manufacturing the desired ASIC" is both contrary to and not supported by the '432 patent's public record as understood by one of skill in the art.

that this step eliminate any selected hardware cells that are not needed. In other words, this generating step "defines the needed hardware cells" by eliminating those hardware cells that have been selected but that are not necessary for the operation of the desired ASIC.

This requirement is also readily apparent from the '432 patent's specification. Specifically, the '432 patent's specification demonstrates that this generating step entails eliminating redundant and unnecessary selected hardware cells. (Ex. 1 at 13:59-66). This is illustrated in FIGS 13, 14, and 15 for the '432 patent. (Ex. 1 at 13:59-66). Given that there may be selected hardware cells that are redundant and/or unnecessary and the netlist defines only needed hardware cells, generating a netlist requires eliminating those unnecessary hardware cells.

Ricoh's opening brief appears to incorrectly claim that this elimination of redundant and unnecessary hardware cells is performed by the selecting step, which in pertinent part provides: "**selecting**…**for each of the specified definitions a corresponding** integrated circuit **hardware cell** for performing the desired function of the application specific integrated circuit, **said step of selecting a hardware cell** comprising **applying to the specified definition of the action or condition to be performed**, a set of **cell selection rules** stored in said expert system knowledge base." Ricoh's argument that these example rules for eliminating redundant and unnecessary hardware cells are encompassed by this selecting step is contrary to the explicit language. Specifically, the "cell selection rules" are "applied" to "each of the specified definitions" and this is done "for selecting a hardware cell" "corresponding" to each of the "specified of the action or condition to be performed." As demonstrated above, this "selecting step" should be interpreted as set forth in N and O of Defendants and Synopsys portion of the Joint Claim Construction Statement.

2. **The Interconnection Requirements To Be Generated For The Netlist Are The Control And Data Paths**

The '432 patent's specification defines the "interconnection requirements" for the necessary hardware cells defined in the netlist as the data and control paths. (Ex. 1 at Abstract; 5:30-35):

> From the flowchart, the system and method uses artificial intelligence and expert system technology to generate a system controller, to select the necessary integrated circuit hardware cells needed to achieve the functional specifications, and to generate **the data and control paths** for the operation of the of the integrated circuit. This list of hardware cells and their **interconnection requirements** is set forth in a netlist.

These portions of the specification reveal that the control and data paths are the "interconnection requirements" that must be generated for the netlist. (*Id*; *See also*, Ex. 1 at FIG. 6; 6:47-54; 13:55-58). Ricoh's claim that the "interconnection requirements" are not the control and data paths but are instead the "necessary parameters for connecting the respective inputs and outputs of each hardware cell" ignores the '432 patent's description and therefore, should be rejected.

3. **A System Controller Must Be Generated For The Netlist**

The claim language "a netlist defining the **hardware cells which are needed"** for the ASIC to be designed and the '432 patent specification unmistakably defines a netlist to include all of the necessary hardware cells and a controller type hardware cell is one of those necessary hardware cells. (Ex. 1 at 4:39-43; 13:67-14:3). Moreover, the Field and Background of the Invention section of the specification also demonstrates that for the netlists in the field of the invention that in addition to defining the hardware components for the ASICs desired function and their interconnection requirements a "system controller must also be designed for synchronizing the operations of these components." (*Id.* at 1:26-28).

Besides the fact that both the claim language and the specification reveal that a netlist requires a controller for controlling the other necessary hardware cells, the requirement that a controller be generated is also supported by the '432 patent's file history. Specifically, the file history limits the input specification by excluding register-transfer level descriptions that would define the control for the hardware cells of the ASIC. (Ex. 4, April 1989 Amendment at 9, November 1989 amendment at 7). Because no control is defined by the claimed invention's input, a controller must be generated to provide any necessary control for the ASIC. (Kowalski at ¶ 61-62). Thus, contrary to Ricoh's arguments, the '432 patent's public record requires that a netlist include a controller type hardware cell and that such a controller must be generated by this generating step in claim 13. This requirement in the '432 patent cannot be overcome by Ricoh's argument that generation of a controller is recited in a dependent claim. *O.I. Corp. v. Tekmar Co.*, 115 F.3d 1576, 1582 (Fed. Cir. 1997) (concluding that where patent description provides clear meaning it trumps doctrine of claim differentiation).

G. **"Generating…Mask Data Required To Produce An Integrated Circuit…"**

The '432 patent defines "mask data" as "the detailed layout level geometrical information." (Ex. 1 at FIG. 1c; Abstract; 1:38-42; 2:44-49).[14] The illustration of mask data in Figure 1c of the '432 patent is also consistent with this definition. (Ex. 1 at FIG. 1c). Thus, the '432 patent demonstrates that "mask data" is the layout level design information generated from the netlist.

The '432 patent provides that "mask data" is "required to produce the particular application specific integrated circuit in chip form." (Ex. 1 at 2:48-49). This is consistent with the understanding of persons of skill in the art that "mask data" is used to manufacture the photomasks (or masks) that are themselves used in the other processes that manufacture the desired ASIC. (Kowalski Decl. ¶¶ 8-9, 65-66). In other words, because the processes that manufacture the desired ASIC require the photomasks, the mask data that is used to manufacture the photomasks is required for producing the ASIC. (*Id.*).

But while layout design information such as mask data is required for producing ASICs, it is certainly not used to directly manufacture ASICs as Ricoh claims. (*Id*. at ¶ 7-10). Ricoh seeks to add the phrase "which can be directly used by a chip foundry in the fabrication of the ASIC." This phrase, however, is contrary to how one of skill in the art would understand "mask data" and also finds no support in the '432 patent or its file history. Thus, the court should adopt Synopsys' and Defendants' proposed construction for claim 14.

H. **The Proper Construction Of Dependent Claims 15-17**

First, for claims 15 and 17, Ricoh again proposes a definition that seeks to obfuscate the distinction between "manufacturing" and "designing." Specifically, Ricoh's proposed interpretation for these two claims includes the phrase "producing signal lines for carrying." (Kowalski Decl. at ¶

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[14] Although dependent claim 14 adds the step of generating mask data from the netlist produced by independent claim 13, from the '432 patent's description it is plain that the KBSC software is not capable of performing that step. (Ex. 1 at 2:57-62). Instead, the '432 patent simply states that there are commercially available computer-aided design systems for producing mask data from the netlist data. (Ex. 1 at 2:44-49, 4:44-46, 5:40-44). Thus, the '432 patent fails to describe any embodiment for creating mask data and this failure renders claim 14 invalid pursuant to 35 U.S.C. § 112.

68 and 72). This phrase finds no support in the '432 patent or its file history. (Ex. 1, Ex. 4). It is also contrary to how one of ordinary skill in the art would interpret claims 15 and 17 because a person of skill in the art would interpret the control and data paths as the interconnection requirements for the hardware cells at the structural level. (Kowalski Decl. at ¶¶ 63-64, 67-68, 71-72; Ex. 1 at Abstract, Figs. 6 & 13-15, 1:17-37; 2:39-44; 3:23-25; 3:40-45; 4:39-43; 5:8-12; 5:30-40; 13:55-14:3). Ricoh claims that the control and data paths are "signal lines" as opposed to "structural descriptions" as proposed by Synopsys and Defendants. Ricoh is wrong. Ricoh supports this claim by relying on only a portion of the description in the '432 patent relating to FIG. 1b. (Ex. 1 at 3:59-65). But the *entire* portion of this section of the '432 patent, however, reveals that it actually supports Synopsys' and Defendants' position that these control and data paths are "structural descriptions" not "signal lines." (*Id.; see also Id.* 3:4-5).

Second, claim 16 requires using a rule-based expert system software including an inference engine for selectively applying the set of IF-THEN rules stored in the knowledge base for generating the data paths for the selected hardware cells. (Kowalski Decl. at ¶ 69-70). Similar to the selecting step of claim 13, Ricoh proposes an interpretation for this claim to eliminate the arguments for the substantial differences between rule-based expert system software and the conventional software programs. This is contrary to the '432 patent and its file history as well as how one of ordinary skill in the art would interpret this claim. (Ex. 1 at Abstract, 5:8-12; 13:55-14:3; Ex. 4, November 1989 Amendment at 7 and 9, Kowalski Decl. at ¶ 69-70).

VI. CONCLUSION

For all of the foregoing reasons and the intrinsic and extrinsic evidence identified in Synopsys' and Defendants' portion of the Joint Claim Construction Statement filed on July 16, 2004, the Court should adopt Synopsys' and Defendants' claim constructions for the '432 patent as set forth in their proposed order filed with this brief.

Dated: September 14, 2004

Respectfully submitted,

By: /s/ Thomas C. Mavrakakis
Thomas C. Mavrakakis
Attorneys for Plaintiff SYNOPSYS, INC., and Defendants AEROFLEX INCORPORATED, et al.

EXHIBIT 8

United States Patent [19]

Kobayashi et al.

[11] **Patent Number: 4,922,432**

[45] **Date of Patent: May 1, 1990**

[54] **KNOWLEDGE BASED METHOD AND APPARATUS FOR DESIGNING INTEGRATED CIRCUITS USING FUNCTIONAL SPECIFICATIONS**

[75] Inventors: **Hideaki Kobayashi**, Columbia, S.C.; **Masahiro Shindo**, Osaka, Japan

[73] Assignees: **International Chip Corporation**, Columbia, S.C.; **Ricoh Company, Ltd.**, Tokyo, Japan

[21] Appl. No.: **143,821**

[22] Filed: **Jan. 13, 1988**

[51] **Int. Cl.**[5] **G06F 15/60**

[52] **U.S. Cl.** **364/490**; 364/489; 364/488; 364/521

[58] **Field of Search** 364/488–491, 364/521, 300, 513

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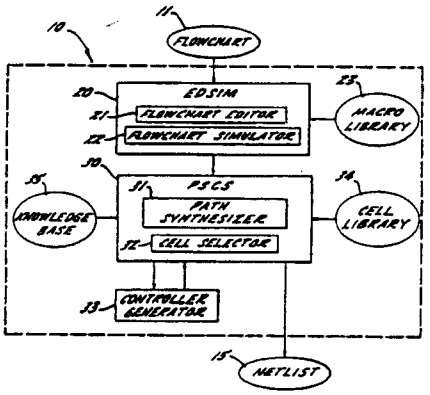
Primary Examiner—Felix D. Gruber
Assistant Examiner—V. N. Trans
Attorney, Agent, or Firm—Bell, Seltzer, Park & Gibson

[57] **ABSTRACT**

The present invention provides a computer-aided design system and method for designing an application specific integrated circuit which enables a user to define functional architecture independent specifications for the integrated circuit and which translates the functional architecture independent specifications into the detailed information needed for directly producing the integrated circuit. The functional architecture independent specifications of the desired integrated circuit can be defined at the functional architecture independent level in a flowchart format. From the flowchart, the system and method uses artificial intelligence and expert systems technology to generate a system controller, to select the necessary integrated circuit hardware cells needed to achieve the functional specifications, and to generate data and control paths for operation of the integrated circuit. This list of hardware cells and their interconnection requirements is set forth in a netlist. From the netlist it is possible using known manual techniques or existing VLSI CAD layout systems to generate the detailed chip level topological information (mask data) required to produce the particular application specific integrated circuit.

20 Claims, 12 Drawing Sheets



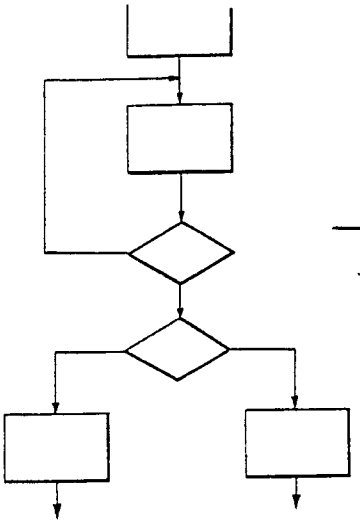


Fig. 1a.
FUNCTIONAL LEVEL

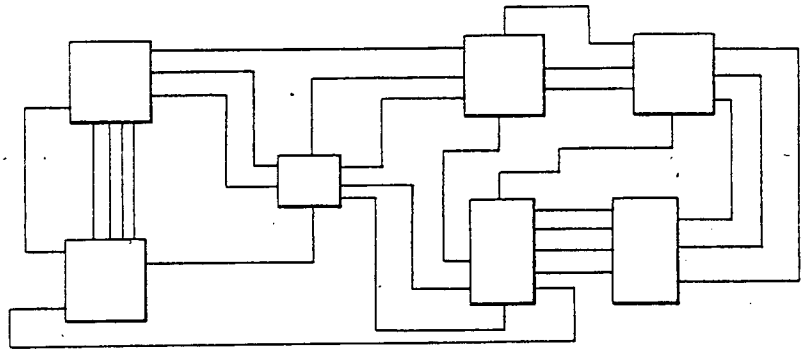


Fig. 1b.
STRUCTURAL LEVEL

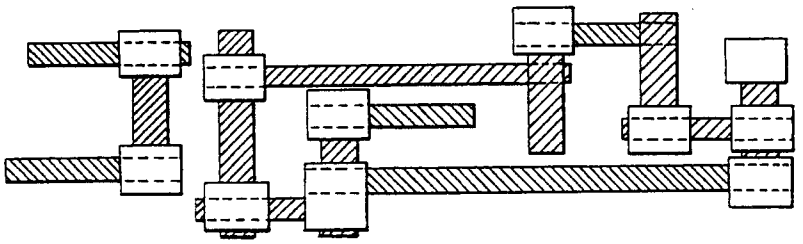


Fig. 1c.
PHYSICAL LAYOUT LEVEL

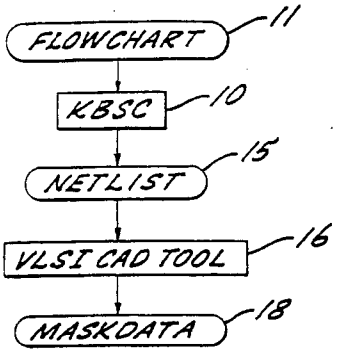

FLOWCHART
11
KBSC
10
NETLIST
15
VLSI CAD TOOL
16
MASKDATA
18

Fig. 2.

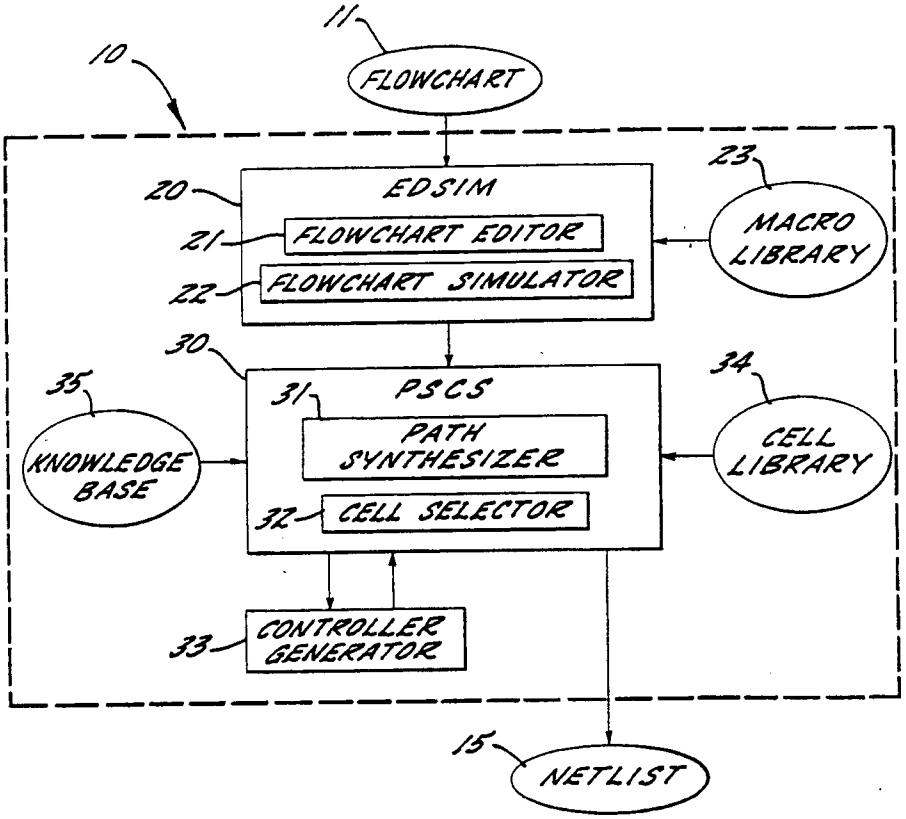

11
FLOWCHART
10
EDSIM
20
FLOWCHART EDITOR
21
FLOWCHART SIMULATOR
22
23
MACRO LIBRARY
30
PSCS
31
PATH SYNTHESIZER
32
CELL SELECTOR
33
CONTROLLER GENERATOR
35
KNOWLEDGE BASE
34
CELL LIBRARY
15
NETLIST

Fig. 3.

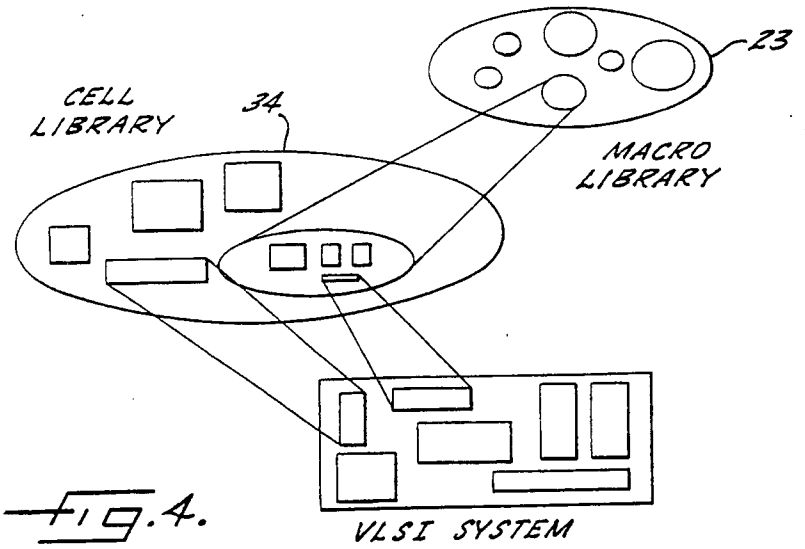

23
CELL LIBRARY
34
MACRO LIBRARY
VLSI SYSTEM

Fig. 4.

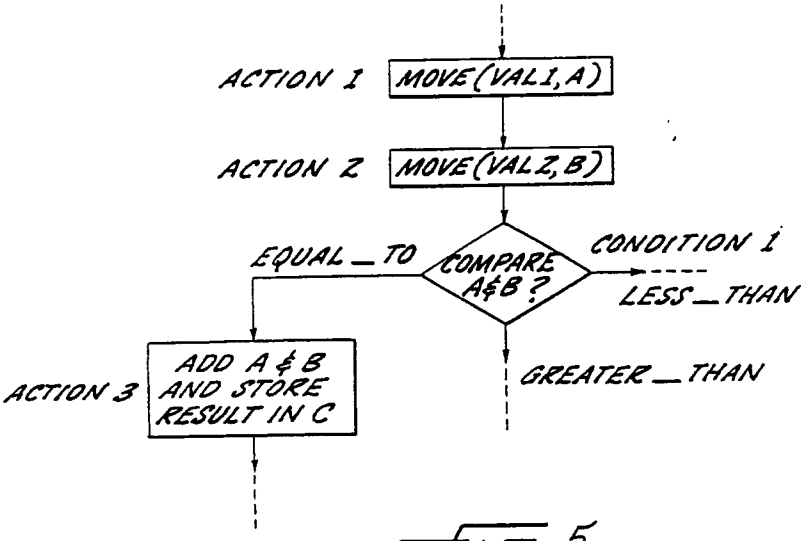

ACTION 1
MOVE(VAL1,A)
ACTION 2
MOVE(VAL2,B)
EQUAL_TO
COMPARE A&B ?
CONDITION 1
LESS_THAN
GREATER_THAN
ACTION 3
ADD A & B AND STORE RESULT IN C

Fig. 5.

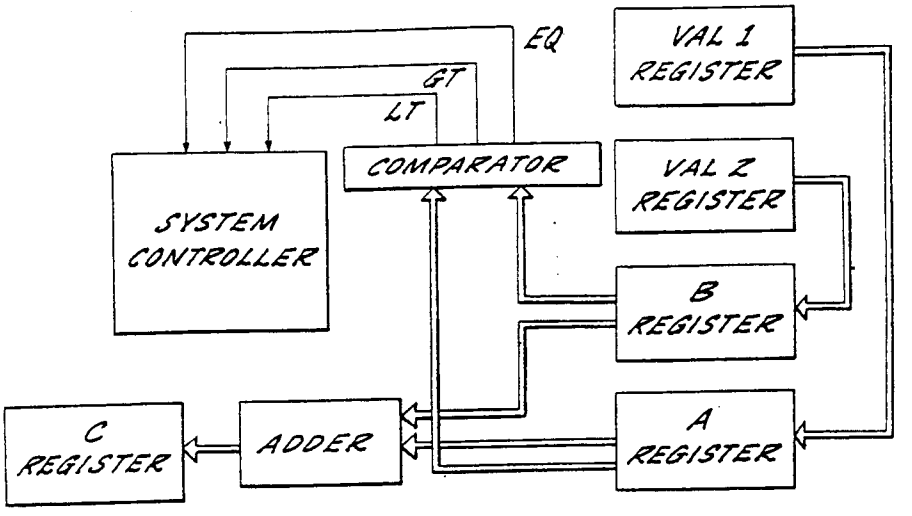

EQ
GT
LT
VAL 1 REGISTER
COMPARATOR
VAL 2 REGISTER
SYSTEM CONTROLLER
B REGISTER
C REGISTER
ADDER
A REGISTER

Fig. 6.

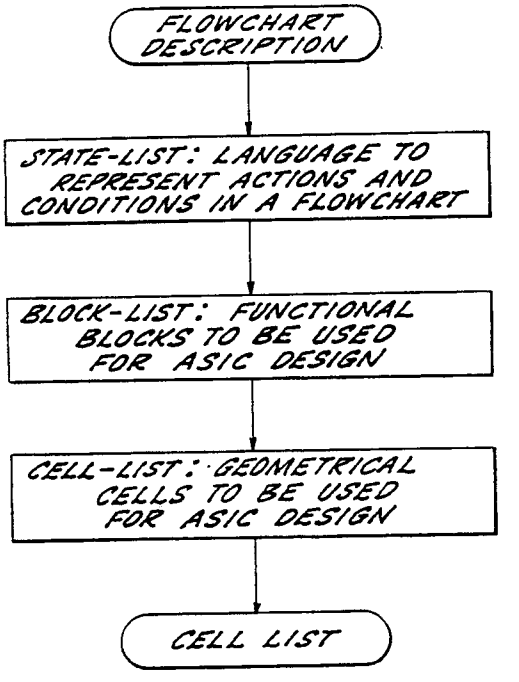

FLOWCHART DESCRIPTION
STATE-LIST: LANGUAGE TO REPRESENT ACTIONS AND CONDITIONS IN A FLOWCHART
BLOCK-LIST: FUNCTIONAL BLOCKS TO BE USED FOR ASIC DESIGN
CELL-LIST: GEOMETRICAL CELLS TO BE USED FOR ASIC DESIGN
CELL LIST

Fig. 9.

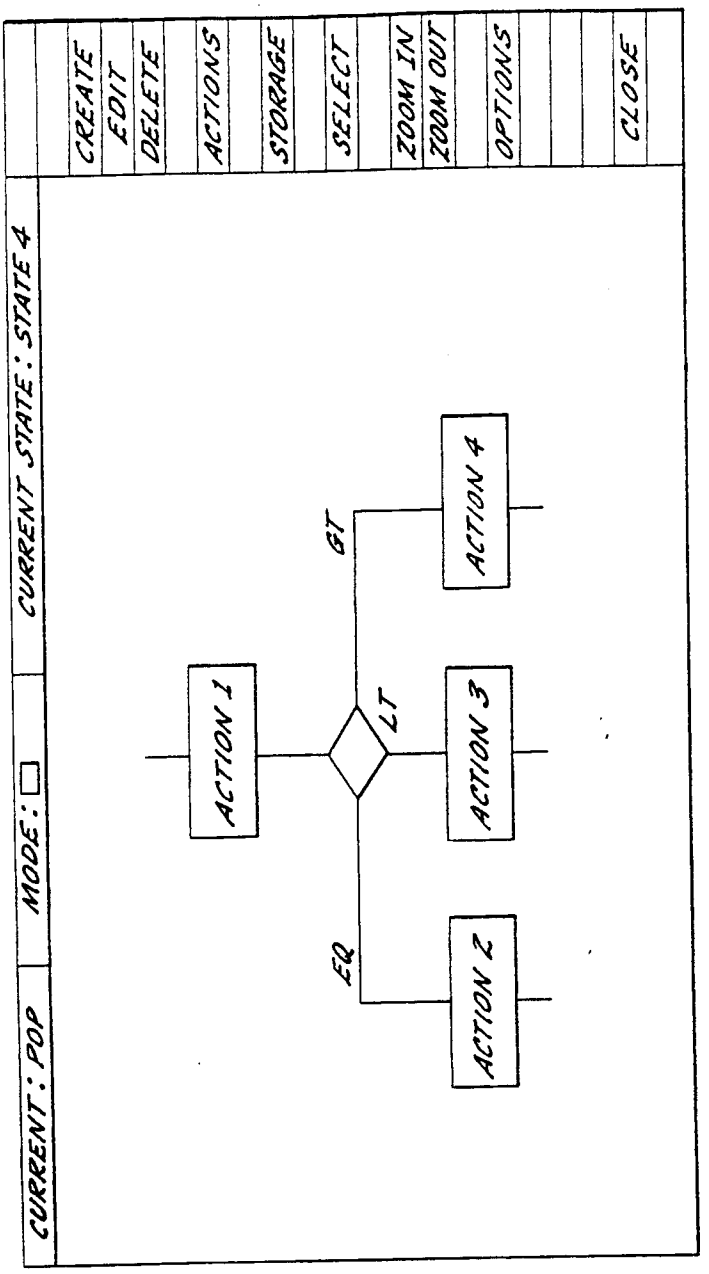

CREATE
EDIT
DELETE
ACTIONS
STORAGE
SELECT
ZOOM IN
ZOOM OUT
OPTIONS
CLOSE
CURRENT STATE: STATE 4
MODE: □
CURRENT: POP
ACTION 1
GT
LT
EQ
ACTION 4
ACTION 3
ACTION 2

FIG. 7.

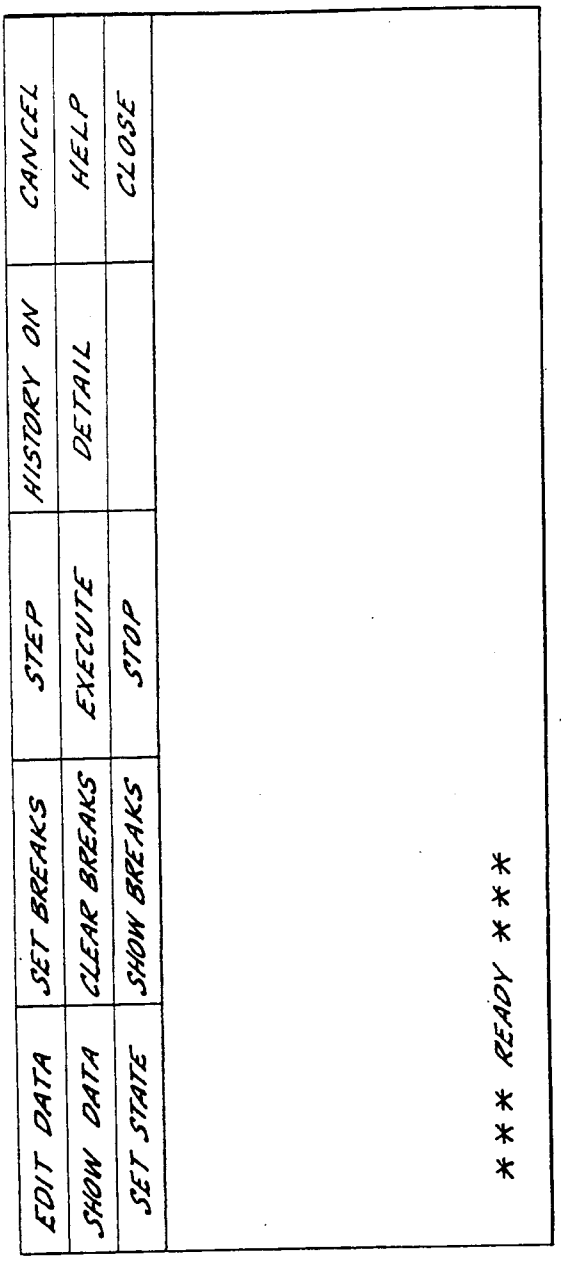

EDIT DATA
SET BREAKS
STEP
HISTORY ON
CANCEL
SHOW DATA
CLEAR BREAKS
EXECUTE
DETAIL
HELP
SET STATE
SHOW BREAKS
STOP
CLOSE
**** READY ****

FIG. 8.

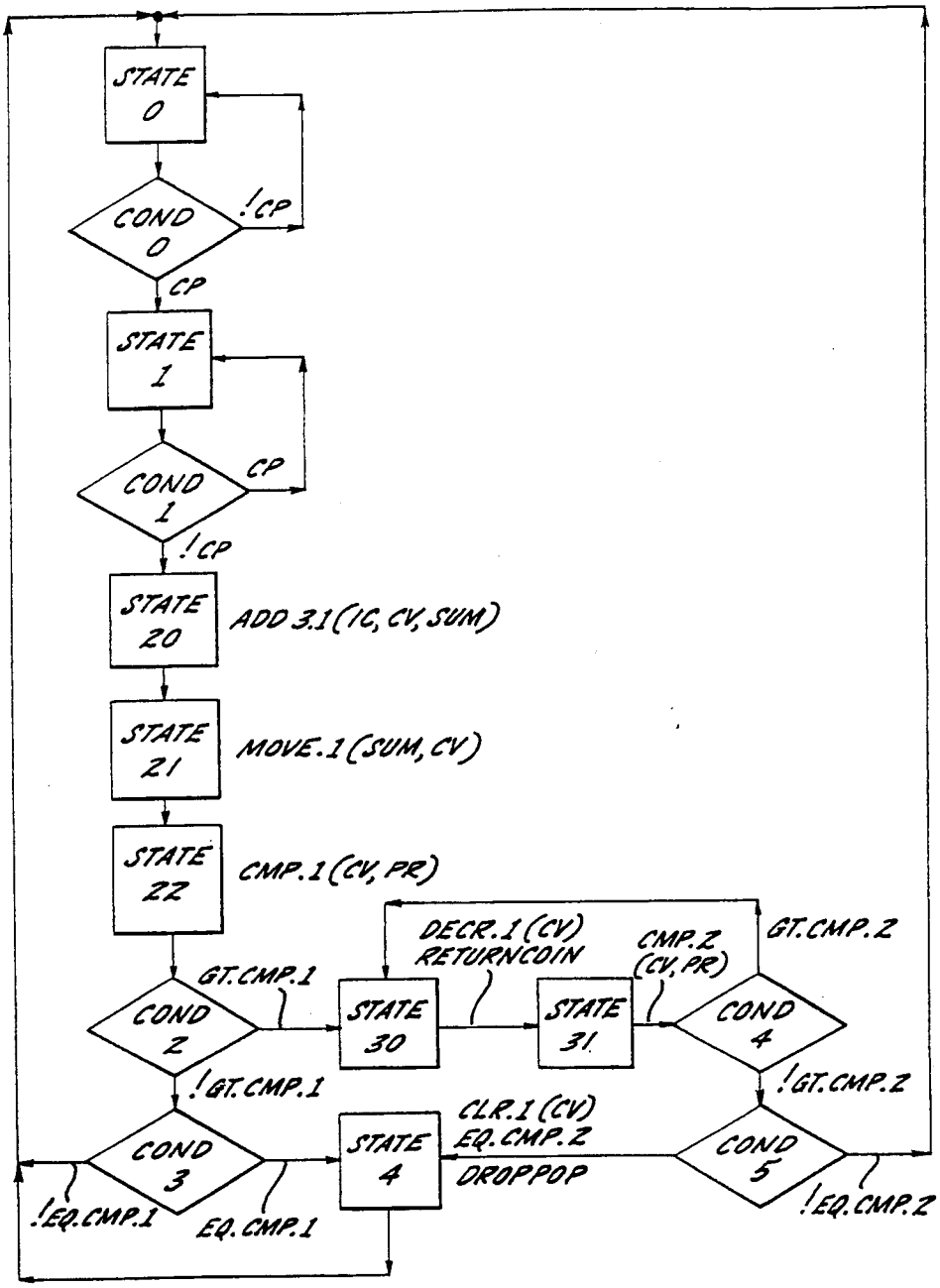

STATE 0
COND 0
!CP
CP
STATE 1
COND 1
CP
!CP
STATE 20
ADD 3.1 (IC, CV, SUM)
STATE 21
MOVE.1 (SUM, CV)
STATE 22
CMP.1 (CV, PR)
GT.CMP.1
COND 2
!GT.CMP.1
STATE 30
DECR.1 (CV)
RETURNCOIN
STATE 31
CMP.2 (CV, PR)
GT.CMP.2
COND 4
!GT.CMP.2
COND 3
!EQ.CMP.1
EQ.CMP.1
STATE 4
CLR.1 (CV)
EQ.CMP.2
DROPPOP
COND 5
!EQ.CMP.2

Fig. 10.

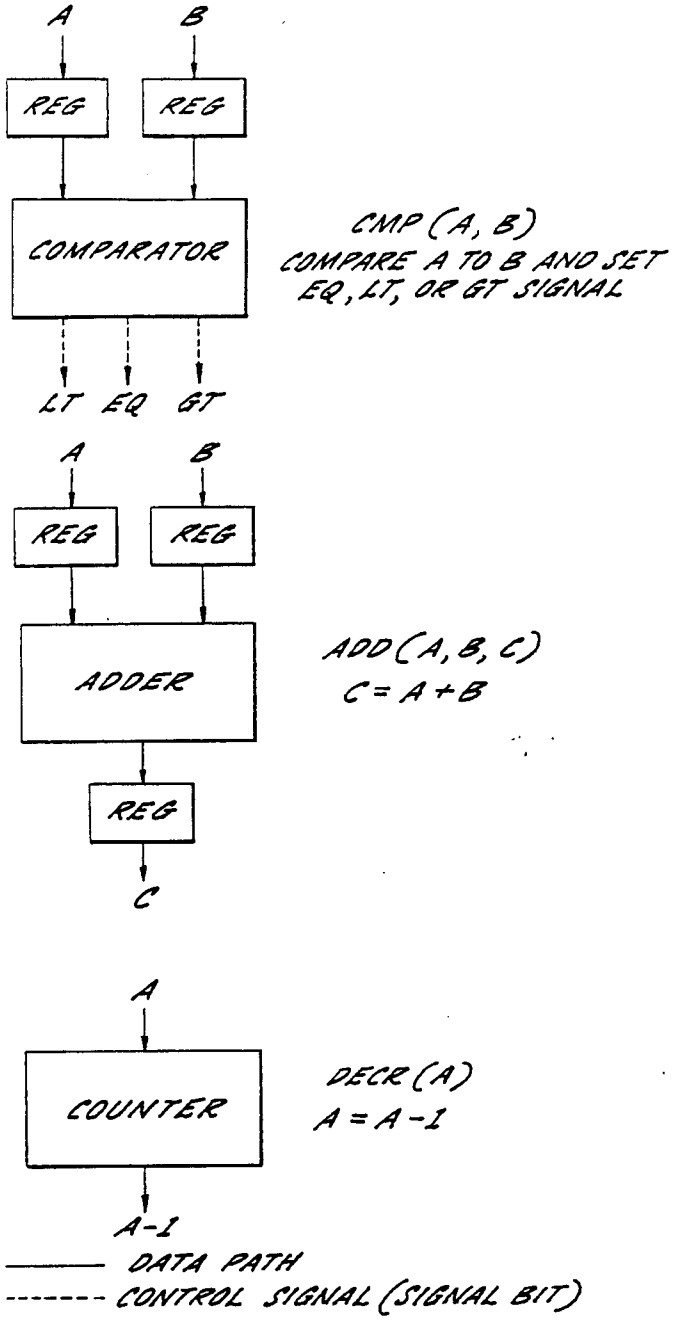

A
B
REG
REG
COMPARATOR
CMP (A, B)
COMPARE A TO B AND SET
EQ, LT, OR GT SIGNAL
LT
EQ
GT
A
B
REG
REG
ADDER
ADD (A, B, C)
C = A + B
REG
C
A
COUNTER
DECR (A)
A = A - 1
A-1
DATA PATH
CONTROL SIGNAL (SIGNAL BIT)

Fig. 11.

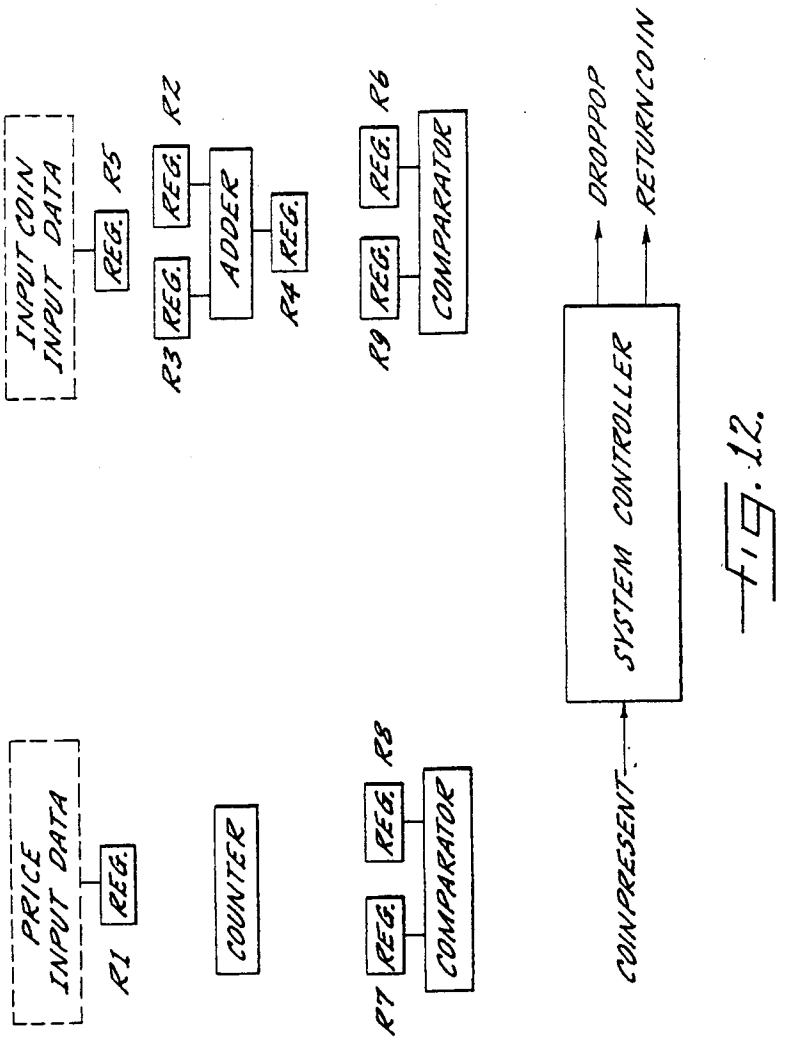

INPUT COIN
INPUT DATA
REG.
R5
REG.
R2
REG.
R3
ADDER
R4
REG.
REG.
R6
REG.
R9
COMPARATOR
DROPPOP
RETURN COIN
SYSTEM CONTROLLER
COINPRESENT
PRICE
INPUT DATA
REG.
R1
COUNTER
REG.
R8
REG.
R7
COMPARATOR

FIG. 12.

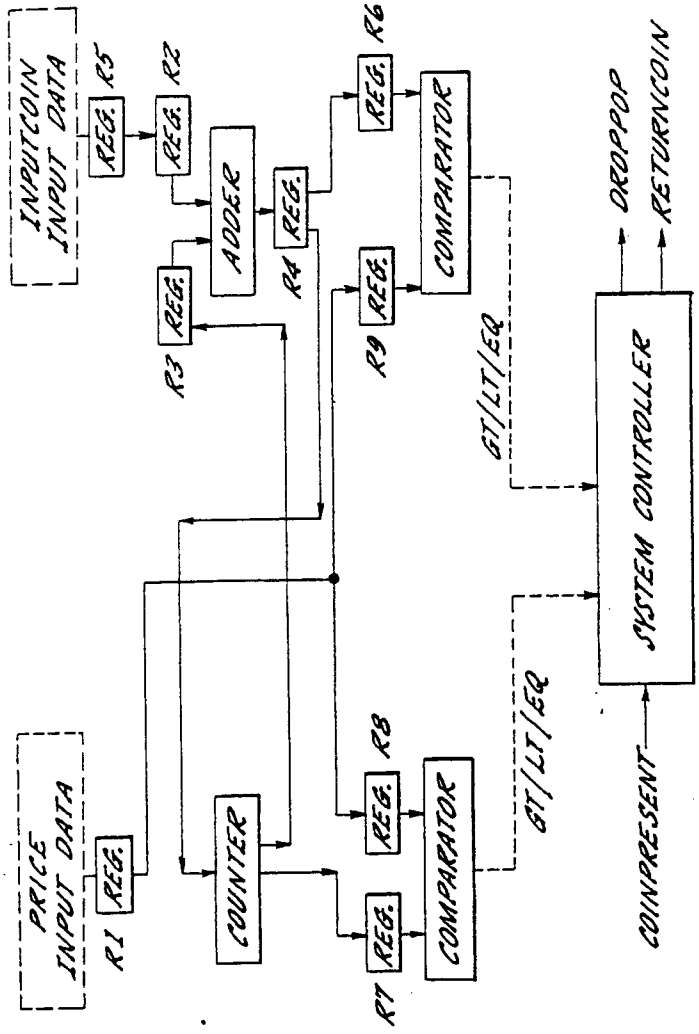

INPUTCOIN INPUT DATA
REG.
R5
REG.
R2
ADDER
REG.
R4
REG.
R6
COMPARATOR
REG.
R3
REG.
R9
GT/LT/EQ
DROPPOP
RETURNCOIN
SYSTEM CONTROLLER
PRICE INPUT DATA
REG.
R1
COUNTER
REG.
R8
REG.
R7
COMPARATOR
GT/LT/EQ
COINPRESENT

FIG. 13.

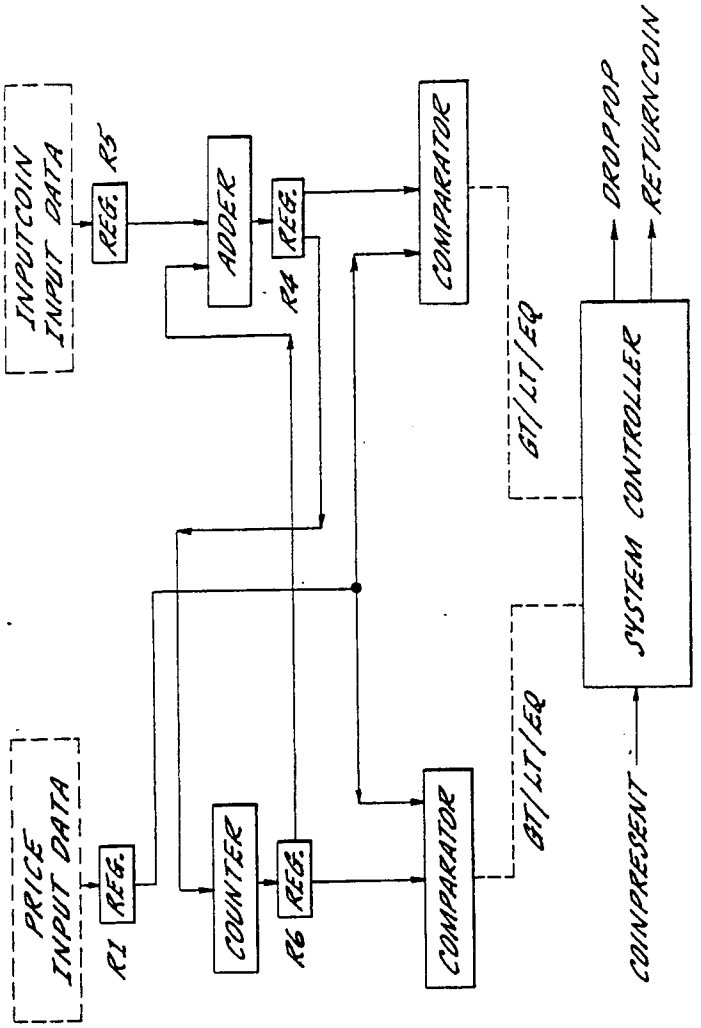

INPUTCOIN INPUT DATA
REG.
R3
ADDER
REG.
R4
COMPARATOR
GT/LT/EQ
DROPPOP
RETURNCOIN
SYSTEM CONTROLLER
PRICE INPUT DATA
REG.
R1
COUNTER
REG.
R6
COMPARATOR
GT/LT/EQ
COINPRESENT

FIG. 14.

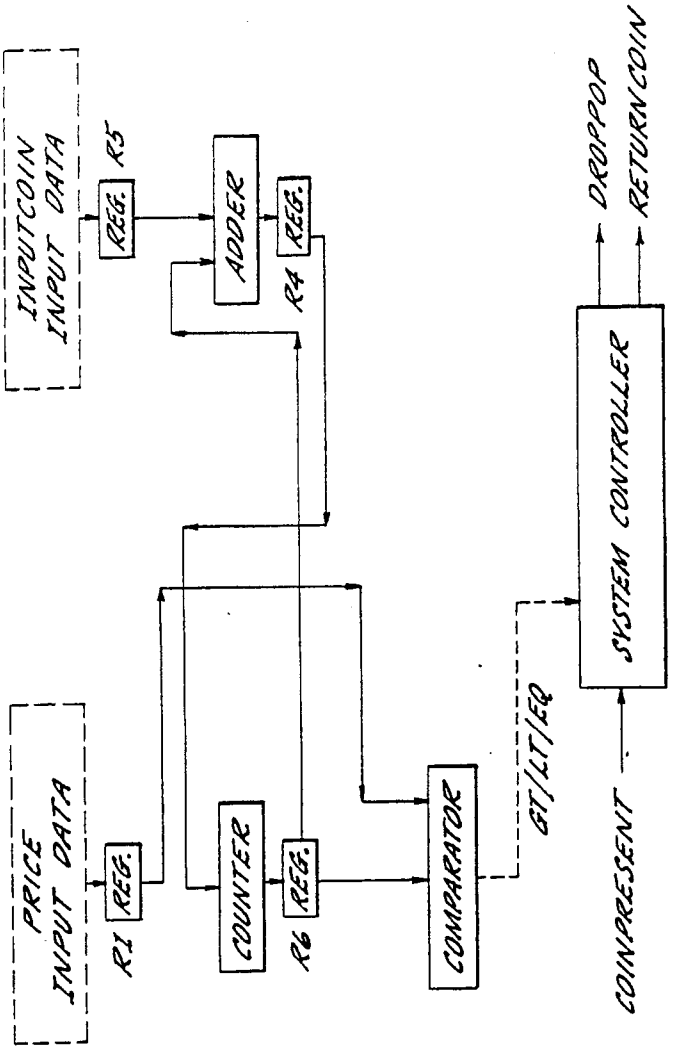

INPUTCOIN
INPUT DATA
REG.
R5
ADDER
REG.
R4
DROPPOP
RETURNCOIN
SYSTEM CONTROLLER
PRICE
INPUT DATA
REG.
R1
COUNTER
REG.
R6
COMPARATOR
GT/LT/EQ
COINPRESENT

Fig. 15.

KNOWLEDGE BASED METHOD AND APPARATUS FOR DESIGNING INTEGRATED CIRCUITS USING FUNCTIONAL SPECIFICATIONS

FIELD AND BACKGROUND OF THE INVENTION

This invention relates to the design of integrated circuits, and more particularly relates to a computer-aided method and apparatus for designing integrated circuits.

An application specific integrated circuit (ASIC) is an integrated circuit chip designed to perform a specific function, as distinguished from standard, general purpose integrated circuit chips, such as microprocessors, memory chips, etc. A highly skilled design engineer having specialized knowledge in VLSI circuit design is ordinarily required to design a ASIC. In the design process, the VLSI design engineer will consider the particular objectives to be accomplished and tasks to be performed by the integrated circuit and will create structural level design specifications which define the various hardware components required to perform the desired function, as well as the interconnection requirements between these components. A system controller must also be designed for synchronizing the operations of these components. This requires an extensive and all encompassing knowledge of the various hardware components required to achieve the desired objectives, as well as their interconnection requirements, signal level compatibility, timing compatibility, physical layout, etc. At each design step, the designer must do tedious analysis. The design specifications created by the VLSI design engineer may, for example, be in the form of circuit schematics, parameters or specialized hardware description languages (HDLs).

From the structural level design specifications, the description of the hardware components and interconnections is converted to a physical chip layout level description which describes the actual topological characteristics of the integrated circuit chip. This physical chip layout level description provides the mask data needed for fabricating the chip.

Due to the tremendous advances in very large scale integration (VLSI) technology, highly complex circuit systems are being built on a single chip. With their complexity and the demand to design custom chips at a faster rate, in large quantities, and for an ever increasing number of specific applications, computer-aided design (CAD) techniques need to be used. CAD techniques have been used with success in design and verification of integrated circuits, at both the structural level and at the physical layout level. For example, CAD systems have been developed for assisting in converting VLSI structural level descriptions of integrated circuits into the physical layout level topological mask data required for actually producing the chip. Although the presently available computer-aided design systems greatly facilitate the design process, the current practice still requires highly skilled VLSI design engineers to create the necessary structural level hardware descriptions.

There is only a small number of VLSI designers who possess the highly specialized skills needed to create structural level integrated circuit hardware descriptions. Even with the assistance of available VLSI CAD tools, the design process is time consuming and the probability of error is also high because of human involvements. There is a very significant need for a better and more cost effective way to design custom integrated circuits.

SUMMARY OF THE INVENTION

In accordance with the present invention a CAD (computer-aided design) system and method is provided which enables a user to define the functional requirements for a desired target integrated circuit, using an easily understood functional architecture independent level representation, and which generates therefrom the detailed information needed for directly producing an application specific integrated circuit (ASIC) to carry out those specific functions. Thus, the present invention, for the first time, opens the possibility for the design and production of ASICs by designers, engineers and technicians who may not possess the specialized expert knowledge of a highly skilled VLSI design engineer.

The functional architecture independent specifications of the desired ASIC can be defined in a suitable manner, such as in list form or preferably in a flowchart format. The flowchart is a highly effective means of describing a sequence of logical operations, and is well understood by software and hardware designers of varying levels of expertise and training. From the flowchart (or other functional specifications), the system and method of the present invention translates the functional architecture independent specifications into structural an architecture specific level definition of an integrated circuit, which can be used directly to produce the ASIC. The structural level definition includes a list of the integrated circuit hardware cells needed to achieve the functional specifications. These cells are selected from a cell library of previously designed hardware cells of various functions and technical specifications. The system also generates data paths among the selected hardware cells. In addition, the present invention generates a system controller and control paths for the selected integrated circuit hardware cells. The list of hardware cells and their interconnection requirements may be represented in the form of a netlist. From the netlist it is possible using either known manual techniques or existing VLSI CAD layout systems to generate the detailed chip level geometrical information (e.g. mask data) required to produce the particular application specific integrated circuit in chip form.

The preferred embodiment of the system and method of the present invention which is described more fully hereinafter is referred to as a Knowledge Based Silicon Compiler (KBSC). The KBSC is an ASIC design methodology based upon artificial intelligence and expert systems technology. The user interface of KBSC is a flowchart editor which allows the designer to represent VLSI systems in the form of a flowchart. The KBSC utilizes a knowledge based expert system, with a knowledge base extracted from expert ASIC designers with a high level of expertise in VLSI design to generate from the flowchart a netlist which describes the selected hardware cells and their interconnection requirements.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood by reference to the detailed description which follows, taken in connection with the accompanying drawings, in which

FIG. 1*a* illustrates a functional level design representation of a portion of a desired target circuit, shown in the form of a flowchart;

FIG. 1*b* illustrates a structural level design representation of an integrated circuit;

FIG. 1*c* illustrates a design representation of a circuit at a physical layout level, such as would be utilized in the fabrication of an integrated circuit chip;

FIG. 2 is a block schematic diagram showing how integrated circuit mask data is created from flowchart descriptions by the KBSC system of the present invention;

FIG. 3 is a somewhat more detailed schematic illustration showing the primary components of the KBSC system;

FIG. 4 is a schematic illustration showing how the ASIC design system of the present invention draws upon selected predefined integrated circuit hardware cells from a cell library;

FIG. 5 is an example flowchart defining a sequence of functional operations to be performed by an integrated circuit;

FIG. 6 is a structural representation showing the hardware blocks and interconnection requirements for the integrated circuit defined in FIG. 5;

FIG. 7 is an illustration of the flowchart editor window;

FIG. 8 is an illustration of the flowchart simulator window;

FIG. 9 is an illustration of the steps involved in cell list generation;

FIG. 10 is an example flowchart for a vending machine system;

FIG. 11 illustrates the hardware components which correspond to each of the three macros used in the flowchart of FIG. 10;

FIG. 12 is an initial block diagram showing the hardware components for an integrated circuit as defined in the flowchart of FIG. 10;

FIG. 13 is a block diagram corresponding to FIG. 12 showing the interconnections between blocks;

FIG. 14 is a block diagram corresponding to FIG. 13 after register optimization; and

FIG. 15 is a block diagram corresponding to FIG. 14 after further optimization.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

FIGS. 1*a*, 1*b* and 1*c* illustrate three different levels of representing the design of an integrated circuit. FIG. 1*a* shows a functional (or behavioral) representation architecture independent in the form of a flowchart. A flowchart is a graphic representation of an algorithm and consists of two kinds of blocks or states, namely actions and conditions (decisions). Actions are conventionally represented in the flowchart by a rectangle or box, and conditions are represented by a diamond. Transitions between actions and conditions are represented by lines with arrows. FIG. 1*b* illustrates a structural (or logic) level representation of an integrated circuit. In this representation, blocks are used to represent integrated architecture specific circuit hardware components for performing various functions, and the lines interconnecting the blocks represent paths for the flow of data or control signals between the blocks. The blocks may, for example, represent hardware components such as adders, comparators, registers, system controllers, etc. FIG. 1*c* illustrates a physical layout level representation of an integrated circuit design, which provides the detailed mask data necessary to actually manufacture the devices and conductors which together comprise integrated circuit.

As noted earlier, the design of an integrated circuit at the structural level requires a design engineer with highly specialized skills and expertise in VLSI design. In the KBSC system of the present invention, however, integrated circuits can be designed at a functional level because the expertise in VLSI design is provided and applied by the invention. Allowing the designer to work with flowcharts instead of logic circuit schematics simplifies the task of designing custom integrated circuits, making it quicker, less expensive and more reliable. The designer deals with an algorithm using simple flowcharts at an architecture independent functional (behavioral) level, and needs to know only the necessary logical steps to complete a task, rather than the specific means for accomplishing the task. Designing with flowcharts requires less work in testing because flowcharts allow the designer to work much closer to the algorithm. On the other hand, previously existing VLSI design tools require the designer to represent an algorithm with complex circuit schematics at a structural level, therefore requiring more work in testing. Circuit schematics make it harder for the designer to cope with the algorithm function which needs to be incorporated into the target design because they intermix the hardware and functional considerations. Using flowcharts to design custom integrated circuits will allow a large number of system designers to access VLSI technology, where previously only a small number of designers had the knowledge and skills to create the necessary structural level hardware descriptions.

The overall system flow is illustrated in FIG. 2. The user enters the functional specifications of the circuit into the knowledge based silicon compiler (KBSC) **10** in the form of a flowchart **11**. The KBSC **10** then generates a netlist **15** from the flowchart. The netlist **15** includes a custom generated system controller, all other hardware cells required to implement the necessary operations, and interconnection information for connecting the hardware cells and the system controller. The netlist can be used as input to any existing VLSI layout and routing tool **16** to create mask data **18** for geometrical layout.

System Overview

The primary elements or modules which comprise the KBSC system are shown in FIG. 3. In the embodiment illustrated and described herein, these elements or modules are in the form of software programs, although persons skilled in the appropriate art will recognize that these elements can easily be embodied in other forms, such as in hardware.

Referring more particularly to FIG. 3, it will be seen that the KBSC system **10** includes a program **20** called EDSIM, which comprises a flowchart editor **21** for creating and editing flowcharts and a flowchart simulator **22** for simulation and verification of flowcharts. Actions to be performed by each of the rectangles represented in the flowchart are selected from a macro library **23**. A program **30** called PSCS (path synthesizer and cell selector) includes a data and control path synthesizer module **31**, which is a knowledge based system for data and control path synthesis. PSCS also includes a cell selector **32** for selecting the cells required for system design. The cell selector **32** selects from a cell

library **34** of previously designed hardware cells the appropriate cell or cells required to perform each action and condition represented in the flowchart. A controller generator **33** generates a custom designed system controller for controlling the operations of the other hardware cells. The knowledge base **35** contains ASIC design expert knowledge required for data path synthesis and cell selection. Thus, with a functional flowchart input, PSCS generates a system controller, selects all other hardware cells, generates data and control paths, and generates a netlist describing all of this design information.

The KBSC system employs a hierarchal cell selection ASIC design approach, as is illustrated in FIG. **4**. Rather than generating every required hardware cell from scratch, the system draws upon a cell library **34** of previously designed, tested and proven hardware cells of various types and of various functional capabilities with a given type. The macro library **23** contains a set of macros defining various actions which can be specified in the flowchart. For each macro function in the macro library **23** there may be several hardware cells in the cell library **34** of differing geometry and characteristics capable of performing the specified function. Using a rule based expert system with a knowledge base **35** extracted from expert ASIC designers, the KBSC system selects from the cell library **34** the optimum cell for carrying out the desired function.

Referring again to FIG. **3**, the cells selected by the cell selector **32**, the controller information generated by the controller generator **33** and the data and control paths generated by the data/control path synthesizer **31** are all utilized by the PSCS program **30** to generate the netlist **15**. The netlist is a list which identifies each block in the circuit and the interconnections between the respective inputs and outputs of each block. The netlist provides all the necessary information required to produce the integrated circuit. Computer-aided design systems for cell placement and routing are commercially available which will receive netlist data as input and will lay out the respective cells in the chip, generate the necessary routing, and produce mask data which can be directly used by a chip foundry in the fabrication of integrated circuits.

System Requirements

The KBSC system can be operated on a suitable programed general purpose digital computer. By way of example, one embodiment of the system is operated in a work station environment such as Sun3 and VAXStation-II/GPX Running UNIX Operating System and X Window Manager. The work station requires a minimum of 8 megabytes of main storage and 20 megabytes of hard disk space. The monitor used is a color screen with 8-bit planes. The software uses C programming language and INGRES relational data base.

The human interface is mainly done by the use of pop up menus, buttons, and a special purpose command language. The permanent data of the integrated circuit design are stored in the data base for easy retrieval and update. Main memory stores the next data temporarily, executable code, design data (flowchart, logic, etc.), data base (cell library), and knowledge base. The CPU performs the main tasks of creating and simulating flowcharts and the automatic synthesis of the design.

Flowchart Example

To describe the mapping of a flowchart to a netlist, consider an example flowchart shown in FIG. **5**, which is of part of a larger overall system. In this illustrative flowchart, two variables, VAL1 and VAL2 are compared and if they are equal, they are added together. In this instance, the first action (Action **1**) involves moving the value of variable VALI to register A. The second action comprises moving the value of variable VAL2 to register B. Condition **1** comprises comparing the values in registers A and B. Action **3** comprises adding the values of registers A and B and storing the result in register C.

In producing an integrated circuit to carry out the function defined in FIG. **5**, the KBSC maps the flowchart description of the behavior of the system to interconnection requirements between hardware cells. The hardware cells are controlled by a system controller which generates all control signals. There are two types of variables involved in a system controller:

(1) Input variables: These are generated by hardware cells, and/or are external input to the controller. These correspond to conditions in the flowchart.

(2) Output variables: These are generated by the system controller and correspond to actions in the flowchart.

FIG. **6** illustrates the results of mapping the flowchart of FIG. **5** onto hardware cells. The actions and the conditions in the flowchart are used for cell selection and data and control path synthesis. The VALI register and VAL2 register and the data paths leading therefrom have already been allocated in actions occurring before Action **1** in our example. Action **1** causes generation of the data register A. Similarly, Action **2** causes the allocation of data register B. The comparator is allocated as a result of the comparison operation in Condition **1**. The comparison operation is accomplished by (1) selecting a comparator cell, (2) mapping the inputs of the comparator cell to registers A and B, (3) generating data paths to connect the comparator with the registers A and B and (4) generating input variables corresponding to equal to, greater than, and less than for the system controller. Similarly the add operation in Action **3** causes selection of the adder cell, mapping of the adder parameters to the registers and creating the data paths.

Following this methodology, a block list can be generated for a given flowchart. This block list consists of a system controller and as many other blocks as may be required for performing the necessary operations. The blocks are connected with data paths, and the blocks are controlled by the system controller through control paths. These blocks can be mapped to the cells selected from a cell library to produce a cell list.

Interactive Flowchart Editor and Simulator

The creation and verification of the flowchart is the first step in the VLSI design methodology. The translation from an algorithm to an equivalent flowchart is performed with the Flowchart Editor **21** (FIG. **3**). The verification of the edited flowchart is performed by the Flowchart Simulator **22** The Flowchart Editor and Simulator are integrated into one working environment for interactive flowchart editing, with a designer friendly interface.

EDSIM is the program which contains the Flowchart Editor **21** and the Flowchart Simulator **22**. It also provides functions such as loading and saving flow-

charts. EDSIM will generate an intermediate file, called a statelist, for each flowchart. This file is then used by the PSCS program **30** to generate a netlist.

Flowchart Editor

The Flowchart Editor **21** is a software module used for displaying, creating, and editing the flowchart. This module is controlled through the flowchart editing window illustrated in FIG. 7. Along with editing functions the Flowchart Editor also provides checking of design errors.

The following is a description of the operations of the Flowchart Editor. The main editing functions include, create, edit, and delete states, conditions, and transitions. The create operation allows the designer to add a new state, condition, or transitions to a flowchart. Edit allows the designer to change the position of a state, condition or transition, and delete allows the designer to remove a state, condition or transition from the current flowchart. States which contain actions are represented by boxes, conditions are represented by diamonds, and transitions are represented by lines with arrows showing the direction of the transition.

Edit actions allows the designer to assign actions to each box. These actions are made up of macro names and arguments. An example of arguments is the setting and clearing of external signals. A list of basic macros available in the macro library **23** is shown in Table 1.

TABLE 1

Macro	Description
ADD (A,B,C)	C = A + B
SUB (A,B,C)	C = A − B
MULT (A,B,C)	C = A * B
DIV (A,B,C)	C = A div B
DECR (A)	A = A − 1
INCR (A)	A = A + 1
CLR (A)	A = 0
REG (A,B)	B = A
CMP (A,B)	Compare A to B and set EQ,LT,GT signals
CMP0 (A)	Compare A to 0 and set EQ,LT,GT signals
NEGATE (A)	A = NOT (A)
MOD (A,B,C)	C = A Modulus B
POW (A,B,C)	C = A B
DC2 (A,S1,S2,S3,S4)	Decode A into S1,S2,S3,S4
EC2 (S1,S2,S3,S4,A)	Encode S1,S2,S3,S4 into A
MOVE (A,B)	B = A
CALL sub-flowchart (A,B, . . .)	Call a sub-flowchart. Pass A,B . . .
START (A,B, . . .)	Beginning state of a sub-flowchart
STOP (A,B . . .)	Ending state of a sub-flowchart

The Flowchart Editor also provides a graphical display of the flowchart as the Flowchart Simulator simulates the flowchart. This graphical display consists of boxes, diamonds, and lines as shown in FIG. 7. All are drawn on the screen and look like a traditional flowchart. By displaying the flowchart on the screen during simulation it allows the designer to design and verify the flowchart at the same time.

Flowchart Simulator

The Flowchart Simulator **22** is a software module used for simulating flowcharts. This module is controlled through the simulator window illustrated in FIG. 8. The Flowchart Simulator simulates the transitions between states and conditions in a flowchart. The following is a list of the operations of the Flowchart Simulator:

edit data—Change the value of a register or memory.
set state—Set the next state to be simulated.
set detail or summary display—Display summary or detail information during simulation.
set breaks—Set a breakpoint.
clear breaks—Clear all breakpoints.
show breaks—Display current breakpoints.
step—Step through one transition.
execute—Execute the flowchart.
stop—Stop executing of the flowchart. history ON or history OFF—Set history recording on or off.
cancel—Cancel current operation.
help—Display help screen.
close—Close the simulator window.

The results of the simulation are displayed within the simulator window. Also the editor window will track the flowchart as it is being simulated. This tracking of the flowchart makes it easy to edit the flowchart when an error is found.

Cell Selection

The Cell Selector **32** is a knowledge based system for selecting a set of optimum cells from the cell library **34** to implement a VLSI system. The selection is based on functional descriptions in the flowchart, as specified by the macros assigned to each action represented in the flowchart. The cells selected for implementing a VLSI system depend on factors such as cell function, fabrication technology used, power limitations, time delays etc. The cell selector uses a knowledge base extracted from VLSI design experts to make the cell selection.

To design a VLSI system from a flowchart description of a user application, it is necessary to match the functions in a flowchart with cells from a cell library. This mapping needs the use of artificial intelligence techniques because the cell selection process is complicated and is done on the basis of a number of design parameters and constraints. The concept used for cell selection is analogous to that used in software compilation. In software compilation a number of subroutines are linked from libraries. In the design of VLSI systems, a functional macro can be mapped to library cell.

FIG. **4** illustrates the concept of hierarchical cell selection. The cell selection process is performed in two steps:

(1) selection of functional macros
(2) selection of geometrical cells

A set of basic macros is shown in Table 1. A macro corresponds to an action in the flowchart. As an example, consider the operation of adding A and B and storing the result in C. This function is mapped to the addition macro ADD(X, Y, Z). The flowchart editor and flowchart simulator are used to draw the rectangles, diamonds and lines of the flowchart, to assign a macro selected from the macro library **23** to each action represented in the flowchart, and to verify the functions in flowcharts. The flowchart is converted into an intermediate form (statelist) and input to the Cell Selector.

The Cell Selector uses a rule based expert system to select the appropriate cell or cells to perform each action. If the cell library has a number of cells with different geometries for performing the operation specified by the macro, then an appropriate cell can be selected on the basis of factors such as cell function, process technology used, time delay, power consumption, etc.

The knowledge base of Cell Selector **32** contains information (rules) relating to:

(1) selection of macros
(2) merging two macros

(3) mapping of macros to cells
(4) merging two cells
(5) error diagnostics

The above information is stored in the knowledge base **35** as rules.

Cell List Generation

FIG. **9** shows the cell list generation steps. The first step of cell list generation is the transformation of the flowchart description into a structure that can be used by the Cell Selector. This structure is called the statelist. The blocklist is generated from the statelist by the inference engine. The blocklist contains a list of the functional blocks to be used in the integrated circuit. Rules of the following type are applied during this stage.

map arguments to data paths
map actions to macros
connect these blocks

Rules also provide for optimization and error diagnostics at this level.

The cell selector maps the blocks to cells selected from the cell library **34**. It selects an optimum cell for a block. This involves the formulation of rules for selecting appropriate cells from the cell library. Four types of information are stored for each cell. These are:

(1) functional level information: description of the cell at the register transfer level.

(2) logic level information: description in terms of flip-flops and gates.

(3) circuit level information: description at the transistor level.

(4) Layout level information: geometrical mask level specification.

The attributes of a cell are:

cell name
description
function
width
height
status
technology
minimum delay
typical delay
maximum delay
power
file
designer
date
comment
inspector

In the cell selection process, the above information can be used. Some parameters that can be used to map macros to cells are:

(1) name of macro
(2) function to be performed
(3) complexity of the chip
(4) fabrication technology
(5) delay time allowed
(6) power consumption
(7) bit size of macro data paths

Netlist Generation

The netlist is generated after the cells have been selected by PSCS. PSCS also uses the macro definitions for connecting the cell terminals to other cells. PSCS uses the state-to-state transition information from an intermediate form representation of a flowchart (i.e. the statelist) to generate a netlist. PSCS contains the following knowledge for netlist generation:

(1) Data path synthesis
(2) Data path optimization
(3) Macro definitions
(4) Cell library
(5) Error detection and correction

The above information is stored in the knowledge base **35** as rules. Knowledge engineers help in the formulation of these rules from ASIC design experts. The macro library **23** and the cell library **34** are stored in a database of KBSC.

A number of operations are performed by PSCS. The following is a top level description of PSCS operations:

(1) Read the flowchart intermediate file and build a statelist.
(2) current_context=START
(3) Start the inference engine and load the current context rules.
(4) Perform one of the following operations depending upon current_context:
(a) Modify the statelist for correct implementation.
(b) Create blocklist, macrolist and data paths.
(c) Optimize blocklist and datapath list and perform error checks.
(d) Convert blocks to cells.
(e) Optimize cell list and perform error checks.
(f) Generate netlist.
(g) Optimize netlist and perform error checks and upon completion Goto 7.
(5) If current_context has changed, load new context rules.
(6) Goto **4**.
(7) Output netlist file and stf files and Stop.

In the following sections, operations mentioned in step 4 are described. The Rule Language and PSCS display are also described.

Rule Language

The rule language of PSCS is designed to be declarative and to facilitate rule editing. In order to make the expert understand the structure of the knowledge base, the rule language provides means for knowledge representation. This will enable the format of data structures to be stated in the rule base, which will enable the expert to refer to them and understand the various structures used by the system. For example, the expert can analyze the structure of wire and determine its components. The expert can then refer these components into rules. If a new object has to be defined, then the expert can declare a new structure and modify some existing structure to link to this new structure. In this way, the growth of the data structures can be visualized better by the expert. This in turn helps the designer to update and append rules.

The following features are included in the rule language:

(i) Knowledge representation in the form of a record structure.
(ii) Conditional expressions in the antecedent of a rule.
(iii) Facility to create and destroy structure in rule actions.
(iv) The assignment statement in the action of a rule.
(v) Facility for input and output in rule actions.
(vi) Provide facility to invoke C functions from rule actions.

The rule format to be used is as follows:

The rule format to be used is as follows:		
Rule	<number> <context>	
If {		
	<if-clause>	
}		
Then	{	
	<then-clause>	
}		
where	<number>	rule number
	<context>	context in which this rule is active
	<if-clause>	the condition part of the rule
	<then-clause>	the action part of the rule

Inference Strategy

The inference strategy is based on a fast pattern matching algorithm. The rules are stored in a network and the requirement to iterate through the rules is avoided. This speeds up the execution. The conflict resolution strategy to be used is based on the following:

(1) The rule containing the most recent data is selected.

(2) The rule which has the most complex condition is selected.

(3) The rule declared first is selected.

Rule Editor

PSCS provides an interactive rule editor which enables the expert to update the rule set. The rules are stored in a database so that editing capabilities of the database package can be used for rule editing. To perform this operation the expert needs to be familiar with the various knowledge structures and the inferencing process. If this is not possible, then the help of a knowledge engineer is needed.

PSCS provides a menu from which various options can be set. Mechanisms are provided for setting various debugging flags and display options, and for the overall control of PSCS.

Facility is provided to save and display the blocklist created by the user. The blocklist configuration created by the user can be saved in a file and later be printed with a plotter. Also the PSCS display can be reset to restart the display process.

PSCS Example Rules:		
Rule 1		
	IF	no blocks exist
	THEN	generate a system controller.
Rule 2		
	IF	a state exists which has a macro AND this macro has not been mapped to a block
	THEN	find a corresponding macro in the library and generate a block for this macro.
Rule 3		
	IF	there is a transition between two states AND there are macros in these states using the same argument
	THEN	make a connection from a register corresponding to the first macro to another register corresponding to the second macro.
Rule 4		
	IF	a register has only a single connection from another register
	THEN	combine these registers into a single register.
Rule 5		
	IF	there are two comparators AND input data widths are of the same size AND one input of these is same AND the outputs of the comparators are used to perform the same operation.
	THEN	combine these comparators into a single comparator.
Rule 6		
	IF	there is a data without a register
	THEN	allocate a register for this data.
Rule 7		
	IF	all the blocks have been interconnected AND a block has a few terminals not connected
	THEN	remove the block and its terminals, or issue an error message.
Rule 8		
	IF	memory is to be used, but a block has not been created for it
	THEN	create a memory block with data, address, read and write data and control terminals.
Rule 9		
	IF	a register has a single connection to a counter
	THEN	combine the register and the counter; remove the register and its terminals.
Rule 10		
	IF	there are connections to a terminal of a block from many different blocks
	THEN	insert a multiplexor; remove the connections to the terminals and connect them to the input of the multiplexor; connect the output of the multiplexor to the input of the block.

Additional rules address the following points:

remove cell(s) that can be replaced by using the outputs of other cell(s)

reduce multiplexor trees

use fan-out from the cells, etc.

Soft Drink Vending Machine Controller Design Example

The following example illustrates how the previously described features of the present invention are employed in the design of an application specific integrated circuit (ASIC). In this illustrative example the ASIC is designed for use as a vending machine controller. The vending machine controller receives a signal each time a coin has been deposited in a coin receiver. The coin value is recorded and when coins totalling the correct amount are received, the controller generates a signal to dispense a soft drink. When coins totalling more than the cost of the soft drink are received, the controller dispenses change in the correct amount.

This vending machine controller example is patterned after a textbook example used in teaching digital system controller design. See Fletcher, William I., *An Engineering Approach to Digital Design,* Prentice-Hall, Inc., pp. 491-505. Reference may be made to this textbook example for a more complete explanation of this vending machine controller requirements, and for an understanding and appreciation of the complex design procedures prior to the present invention for designing the hardware components for a controller.

FIG. 10 illustrates a flowchart for the vending machine controller system. This flowchart would be entered into the KBSC system by the user through the flowchart editor. Briefly reviewing the flowchart, the controller receives a coin present signal when a coin is received in the coin receiver. State0 and cond0 define a waiting state awaiting deposit of a coin. The symbol CP represents "coin present" and the symbol !CP repre-

sents "coin not present". Statel and condI determine when the coin has cleared the coin receiver. At state20, after receipt of a coin, the macro instruction ADD3.1 (lc, cv, sum) instructs the system to add lc (last coin) and cv (coin value) and store the result as sum. The macro instruction associated with state21 moves the value in the register sum to cv. The macro CMP.1 at state22 compares the value of cv with PR (price of soft drink) and returns signals EQ, GT and LT. The condition cond2 tests the result of the compare operation CMP.1. If the result is "not greater than" (!GT.CMP.1), then the condition cond3 tests to see whether the result is "equal" (EQ.CMP.1). If the result is "not equal" (!EQ.CMP.1), then control is returned to state0 awaiting the deposit of another coin. If cond3 is EQ, then state4 generates a control signal to dispense a soft drink (droppop) and the macro instruction CLR.1(cv) resets cv to zero awaiting another customer.

If the total coins deposited exceed the price, then state30 produces the action "returncoin". Additionally, the macro DECR.1 (cv) reduces the value of cv by the amount of the returned coin. At state31 cv and PR are again compared. If cv is still greater than PR, then control passes to state30 for return of another coin. The condition cond5 tests whether the result of CMP.2 is EQ and will result in either dispensing a drink (droppop) true or branching to state0 awaiting deposit of another coin. The macros associated with the states shown in FIG. 10 correspond to those defined in Table 1 above and define the particular actions which are to be performed at the respective states.

Appendix A shows the intermediate file or "statelist" produced from the flowchart of FIG. 10. This statelist is produced as output from the EDSIM program 20 and is used as input to the PSCS program 30 (FIG. 3).

FIG. 11 illustrates for each of the macros used in the flowchart of FIG. 10, the corresponding hardware blocks. It will be seen that the comparison macro CMP (A,B) results in the generation of a register for storing value A, a register for storing value B, and a comparator block and also produces control paths to the system controller for the EQ, LT, and GT signals generated as a result of the comparison operation. The addition macro ADD (A,B,C) results in the generation of a register for each of the input values A and B, a register for the output value C, and in the generation of an adder block. The macro DECR (A) results in the generation of a counter block. The PSCS program 30 maps each of the macros used in the flowchart of FIG. 10 to the corresponding hardware components results in the generation of the hardware blocks shown in FIG. 12. In generating the illustrated blocks, the PSCS program 30 relied upon rules 1 and 2 of the above listed example rules.

FIG. 13 illustrates the interconnection of the block of FIG. 12 with data paths and control paths. Rule 3 was used by the data/control path synthesizer program 31 in mapping the data and control paths.

FIG. 14 shows the result of optimizing the circuit by applying rule 4 to eliminate redundant registers. As a result of application of this rule, the registers R2, R3, R7, R8, and R9 in FIG. 13 were removed. FIG. 15 shows the block diagram after further optimization in which redundant comparators are consolidated. This optimization is achieved in the PSCS program 30 by application of rule 5.

Having now defined the system controller block, the other necessary hardware blocks and the data and control paths for the integrated circuit, the PSCS program 30 now generates a netlist 15 defining these hardware components and their interconnection requirements. From this netlist the mask data for producing the integrated circuit can be directly produced using available VLSI CAD tools.

```
name rpop;
data path @ic<0:5>, cv<0:5>, sum<0:5>, @pr<0:5>;
{
state4 : state0;
state30 : state31;
state21 : state22;
state20 : state21;
state0 :. !cp state0;
state0 :. cp state1;
state1 :. cp state1;
state1 :. !cp state20;
state22 :. GT.CMP.1 state30;
state22 :. !GT.CMP.1*EQ.CMP.1 state4;
state22 :. !GT.CMP.1*!EQ.CMP.1 state0;
state31 :. GT.CMP.2 state30;
state31 :. !GT.CMP.2*EQ.CMP.2 state4;
state31 :. !GT.CMP.2*!EQ.CMP.2 state0;
state30 :: returncoin;
state30 :: DECR.1(cv);
state4 :: droppop;
state4 :: CLR.1(cv);
state31 :: CMP.2(cv,pr);
state22 :: CMP.1(cv,pr);
state21 :: MOVE.1(sum,cv);
state20 :: ADD3.1(ic,cv,sum);
}
```

That which I claimed is:

1. A computer-aided design system for designing an application specific integrated circuit directly from architecture independent functional specifications for the integrated circuit, comprising

a macro library defining a set of architecture independent operations comprised of actions and conditions;

input specification means operable by a user for defining architecture independent functional specifications for the integrated circuit, said functional specifications being comprised of a series of operations comprised of actions and conditions, said input specification means including means to permit the user to specify for each operation a macro selected from said macro library;

a cell library defining a set of available integrated circuit hardware cells for performing the available operations defined in said macro library;

cell selection means for selecting from said cell library for each macro specified by said input specification means, appropriate hardware cells for performing the operation defined by the specified macro, said cell selection means comprising an expert system including a knowledge base containing rules for. selecting hardware cells from said cell library and inference engine means for selecting appropriate hardware cells from said cell library in accordance with the rules of said knowledge base; and

netlist generator means cooperating with said cell selection means for generating as output from the system a netlist defining the hardware cells which are needed to achieve the functional requirements of the integrated circuit and the connections therebetween.

2. The system as defined in claim 1 wherein said input means comprises means specification for receiving user

input of a list defining the series of actions and conditions.

3. The system as defined in claim 1 additionally including mask data generator means for generating from said netlist the mask data required to produce an integrated circuit having the specified functional requirements.

4. The system as defined in claim 1 wherein said input means comprises flowchart editor means specification for creating a flowchart having elements representing said series of actions and conditions.

5. The system as defined in claim 4 additionally including flowchart simulator means for simulating the functions defined in the flowchart to enable the user to verify the operation of the integrated circuit.

6. The system as defined in claim 1 additionally including data path generator means cooperating with said cell selection means for generating data paths for the hardware cells selected by said cell selection means.

7. The system as defined in claim 6 wherein said data path generator means comprises a knowledge base containing rules for selecting data paths between hardware cells and inference engine means for selecting data paths between the hardware cells selected by said cell selection means in accordance with the rules of said knowledge base and the arguments of the specified macros.

8. The system as defined in claim 6 additionally including control generator means for generating a controller and control paths for the hardware cells selected by said cell selection means.

9. A computer-aided design system for designing an application specific integrated circuit directly from a flowchart defining architecture independent functional requirements of the integrated circuit comprising

a marco library defining a set of architecture independent operations comprised of actions and conditions;

flowchart editor means operable by a user for creating a flowchart having elements representing said architecture independent operations;

said flowchart editor means including macro specification means for permitting the user to specify for each operation represented in the flowchart a macro selected from said macro library;

a cell library defining a set of available integrated circuit hardware cells for performing the available operations defined in said macro library;

cell selection means for selecting form said cell library for each specified macro, appropriate hardware cells for performing the operation defined by the specified macro, said cell selection means comprising an expert system including a knowledge base containing rules for selecting hardware cells from said cell library and inference engine means for selecting appropriate hardware cells from said cell library in accordance with the rules of said knowledge base; and

data path generator means cooperating with said cell selection means for generating data paths for the hardware cells selected by said cell selector means, said data path generator means comprising a knowledge base containing rules for selecting data paths between hardware cells and inference engine means for selecting data paths between hardware cells selected by said cell selection means in accordance with the rules of said knowledge base and the arguments of the specified macros.

10. The system as defined in claim 9 additionally including control generator means for generating a controller and control paths for the hardware cells selected by said cell selection means.

11. A computer-aided design system for designing an application specific integrated circuit directly from a flowchart defining architecture independent functional requirements of the integrated circuit, comprising

flowchart editor means operable by a user for creating a flowchart having boxes representing architecture independent actions, diamonds representing architecture independent conditions, and lines with arrows representing transitions between actions and condition and including means for specifying for each box or diamond, a particular action or condition to be performed;

a cell library defining a set of available integrated circuit hardware cells for performing actions and conditions;

a knowledge base containing rules for selecting hardware cells from said cell library and for generating data and control paths for hardware cells; and

expert system means operable with said knowledge base for translating the flowchart defined by said flowchart editor means into a netlist defining the necessary hardware cells and data and control paths required in an integrated circuit having the specified functional requirements.

12. The system as defined in claim 11 including mask data generator means for generating from said netlist the mask data required to produce an integrated circuit having the specified functional requirements.

13. A computer-aided design process for designing an application specific integrated circuit which will perform a desired function comprising

storing a set of definitions of architecture independent actions and conditions;

storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set;

storing in an expert system knowledge base a set of rules for selecting hardware cells to perform the actions and conditions;

describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions;

specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed; and

selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit, said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base and generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor.

14. A process as defined in claim 13, including generating from the netlist the mask data required to produce an integrated circuit having the desired function.

15. A process as defined in claim 13 including the further step of generating data paths for the selected integrated circuit hardware cells.

16. A process as defined in claim 15 wherein said step of generating data paths comprises applying to the selected cells a set of data path rules stored in a knowledge base and generating the data paths therefrom.

17. A process as defined in claim 16 including the further step of generating control paths for the selected integrated circuit hardware cells.

18. A knowledge based design process for designing an application specific integrated circuit which will perform a desired function comprising

storing in a macro library a set of macros defining architecture independent actions and conditions;

storing in a cell library a set of available integrated circuit hardware cells for performing the actions and conditions;

storing in a knowledge base set of rules for selecting hardware cells from said cell library to perform the actions and conditions defined by the stored macros;

describing for a proposed application specific integrated circuit a flowchart comprised of elements representing a series of architecture independent actions and conditions which carry out the function to be performed by the integrated circuit;

specifying for each described action and condition of said series a macro selected from the macro library which corresponds to the action or condition; and

applying rules of said knowledge base to the specified macros to select from said cell library the hardware cells required for performing the desired function of the application specific integrated circuit and generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor.

19. A process as defined in claim 18 also including the steps of

storing in said knowledge base a set of rules for creating data paths between hardware cells, and

applying rules of said knowledge base to the specified means to create data paths for the selected hardware cells.

20. A process as defined in claim 19 also including the steps of generating a controller and generating control paths for the selected hardware cells.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,922,432

DATED : May 1, 1990

INVENTOR(S) : Hideaki Kobayashi, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

ON TITLE PAGE: under the section "References Cited" under "Other Publications":

"Verifying Compiled Silicon", by E. K. cheng, VLSI Design, Oct. 1984, pp. 1-4." should be -- "Verifying Compiled Silicon", by E. K. Cheng, VLSI Design, Oct. 1984, pp. 1-4." --.

"quality of Designs from An Automatic Logic Generator", by T. D. Friedman et al., IEEE 7th DA Conference, 1970, pp. 71-89." should be -- "Quality of Designs from An Automatic Logic Generator", by T. D. Friedman et al., IEEE 7th DA Conference, 1970, pp. 71-89. --.

"Trevillyan-Trickey, H., Flamel: *A High Level Hardward Compiler*, IEEE Transactions On Computer Aided Design, Mar. 1987, pp. 259-269." should be -- Trevillyan-Trickey, H., Flamel: *A High Level Hardware Compiler*, IEEE Transactions On Computer Aided Design, Mar. 1987, pp. 259-269. --.

In the abstract:

Every occurrence of "functional architecture independent" should be -- architecture independent functional --.

Column 1, line 19, "a" should be -- an --.

[redacted]

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,922,432

DATED : May 1, 1990

INVENTOR(S) : Hideaki Kobayashi, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2, line 10, "functional architecture independent" should be -- architecture independent functional --.

Column 2, line 21, "functional architecture independent" should be -- architecture independent functional --.

Column 2, lines 29-30, "functional architecture independent" should be -- architecture independent functional --.

Column 2, line 31, "structural" should be after "specific".

Column 3, lines 51-52, "representation" should be after "architecture independent".

Column 3, lines 61-62, "integrated" should be after "specific".

Column 6, line 62, after "22" insert -- . --.

Column 7, line 43 (in Table 1), "C = A B" should be -- C = A^B --.

Column 8, line 9 should end with the word "flowchart" and "history" should begin on the next line.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,922,432

DATED : May 1, 1990

INVENTOR(S) : Hideaki Kobayashi, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 10, line 23, "data paths" should be -- datapaths --.

Column 10, line 68, delete "The rule format to be used is as follows:".

Column 12, line 54, "Enqineering" should be -- Engineering --.

Column 13, line 55, "block" should be -- blocks --.

In the Claims:

Column 14, line 68, before "means" (first occurrence) insert -- specification --; after "means" (second occurrence) delete "specification".

Column 15, line 9, before "means" (first occurrence) insert -- specification --; after "means" (second occurrence) delete "specification".

Column 15, line 35, after "circuit" insert -- , --.

Column 15, line 36, "marco" should be -- macro --.

Column 15, line 49, "form" should be -- from --.

[redacted] RCL002953

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,922,432

DATED : May 1, 1990

INVENTOR(S) : Hideaki Kobayashi, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 16, line 14, "condition" should be
-- conditions --.

Column 17, line 19, after "base" insert -- a --.

Signed and Sealed this

Fourteenth Day of January, 1992

Attest:

HARRY F. MANBECK, JR.

Attesting Officer

Commissioner of Patents and Trademarks

EXHIBIT 9

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October 13, 2004

BY FACSIMILE and US Mail

Tom Mavrakakis, Esq.
Howrey Simon Arnold & White LLP
301 Ravenswood Ave.
Menlo Park, CA 94025

Re: Synopsys, Inc. v. Ricoh Company, Ltd.
Ricoh Company, Ltd v. Aeroflex Inc., et al.
Our Ref.: R2180.0171

Dear Tom:

Attached is a revised draft tutorial outline (with redline additions shown in *double* underline). This revised draft includes the non-adversarial points from your September 20, 2004 tutorial draft that arguably were not previously captured by Dr. Soderman's September 20 draft outline.

Very truly yours,

DeAnna Allen

DA/edb
Enclosure

cc: Janna Whitte
Edward Meilman, Esq.

Redline: October 13, 2004

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I. Introduction

A. Dr. Donald A. Soderman

B. **[VISUAL]** Background

1. Education

2. Work Experience

3. Experience in ASIC Industry

II. ASICs

A. **[VISUAL]** ASIC- as described in the '432 patent is a specialized integrated circuit chip "designed to perform a specific function."[1]

B. **[VISUAL]** Non-ASIC- "standard, general purpose integrated circuit chips, such as microprocessors, memory chips, etc."[2]

C. **[VISUAL]** Many products common in today's market use ASICs.

D. **[VISUAL]** ASICs have many advantages over general purpose ICs including, that ASICs are smaller, have lower cost and have higher performance.

III. Evolution of ASIC

A. Around 1980, ASICs were simple circuits that very few people were using and even fewer were designing.

B. **[VISUAL]** "In the design process, the VLSI design engineer will consider the particular objectives to be accomplished and tasks to be performed by the integrated circuit and will create structural level design specifications which define the various hardware components required to perform the desired function, as well as the interconnection requirements between these components."[3]

C. **[VISUAL]** Structural level hardware descriptions are descriptions of the architecture or structure (e.g., logic gates, flip flops, etc.) of the circuit desired to be produced as an ASIC, and an example of such a description can be seen from Fig. 1b of the '432 patent.[4] Frequently this done by implicit or explicit selection of gates.

D. **[VISUAL]** In the late 1980's advances in very large scale integrated (VLSI) circuits allowed more highly complex circuits to be integrated on a single chip. This led to the use of ASICs in rapidly expanding list of specific applications, at a faster

design rate, in larger quantities.[5] This led to the need to resolve the following PROBLEMS:

1. **[VISUAL]** "There is only a small number of VLSI designers who possess the highly specialized skills needed to create structural level integrated circuit hardware descriptions."[6]

2. **[VISUAL]** Even with then existing CAD tools that facilitate parts of the process (i.e., layout design), "the design process is time consuming."[7] For example, using such CAD tools, the manufacture of an ASIC for a video camera could require 9 months to a year for design, and an additional 3 or more months for production. At times, the design portion of the process could take longer than a year and sometimes nearly the life cycle of the ASIC. (The life cycle of any particular ASIC was often only a few years.)

3. **[VISUAL]** "[T]he probability of error is also high because of human involvements"[8] and the cost even greater. Designer's working at the structural level commonly made errors in their design specifications, such as choosing the wrong hardware components for a schematic or drawing the wrong wire connections between hardware components in a schematic. An error in the original design, for example, could require months of redesign effort. Errors often were not detected until product testing, after which the manufacturing team needed to find the error, make the design change, release new mask sets, and produce new wafers.

IV. Overview of Manufacturing

A. **[VISUAL]** The manufacturing process is made up of two parts: design and production.

B. **[VISUAL]** In prior art ASIC design, designers commonly created structural descriptions of the circuit desired to be produced. The individual circuit components described in the structural descriptions (Fig. 1b), however, are not individually assembled and placed on the ASIC. Instead, the component circuitry is built-up in layers of complex patterns of semiconductor material (e.g., silicon dioxide, polysilicon, metal, etc.).

C. **[VISUAL]** From the structural description, ASIC designers would create a physical description (known as a "layout" or "placing") needed to directly produce the ASIC.[9] Layout (or placing) enables a designer to plan the location of the circuit blocks in the design. An exemplary layout representation is shown in Fig. 1c of the '432 patent. The layout representation provides the physical ("geometrical") data needed to produce the ASIC. In particular, the layout is made up of a series of

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"mask" (also known as "photomask") layers or levels. Each "mask" stencils a pattern for a given layer of the ASIC. When taken together, the different circuit patterns (or mask levels) make up the circuitry of the desired ASIC. (The data describing the layout representation is known as "mask data" because it describes the different mask levels used in producing the ASIC.)

D. Production of the ASIC:

1. **[VISUAL]** In the production of ASICs, as with other integrated circuit chips, a piece of semiconductor material is provided as a base or initial layer (known as a "substrate") on which other semiconductor material is then deposited. Typically, the base semiconductor material is silicon. The piece of semiconductor material, silicon for example purposes, is typically in the form of a thinly sliced "wafer".

2. **[VISUAL]** A netlist comprising data describing structural ASIC components is directly used to create the layout for the mask data from which mask level patterns are created. As part of ASIC production, each of the mask level patterns generated from the netlist is transferred to the wafer. Each mask level pattern corresponds to one layer for the components that comprise the ASIC. To produce the ASIC as designed, the silicon wafer is covered with a first layer of material that does not conduct electricity (for example "silicon dioxide"). In order to build a first layer for the ASIC components, light-sensitive material (known as "photoresist") is placed over the silicon dioxide. A first mask level is placed over the wafer and light (typically ultraviolet light) is transmitted through the pattern in the mask level to the photoresist on the wafer. The photoresist is chemically responsive to the light so that selected areas corresponding to the mask level pattern are formed in the photoresist.

3. **[VISUAL]** A process known as "etching" is applied to the photoresist. Etching transfers the mask level pattern in the photoresist so that a corresponding pattern of selected areas are formed in the layer of silicon dioxide below. Based on the pattern formed in the oxide, a layer of semiconductor material for the ASIC components is produced on the ASIC.

4. **[VISUAL]** In order to produce a next layer for the ASIC components, the previous, patterned layer of oxide is removed and replaced with a new, unpatterned oxide layer. A layer of polysilicon and a new layer of photoresist are applied. Using a second mask level pattern, the process repeats the steps of transferring the mask level pattern to the photoresist layer and then to

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the oxide layer to create corresponding selected areas. A second layer of semiconductor material for the ASIC components corresponding to the second mask level is then produced based on the oxide layer pattern. Each subsequent layer of semiconductor material for the ASIC components is produced in a similar manner using the successive mask levels generated from the mask data and netlist.

V. Process Patented in '432 Patent

A. Advantages:

1. **[VISUAL]** The '432 patent's invention is directed to a computer-aided-design ("CAD") system and method for designing ASICs. The patented process simplifies the process of designing and producing ASICs, and makes the process quicker, less expensive, and more reliable. Using the invention, a designer is able to define the ASIC using architectural independent functional descriptions (e.g., functional HDLs (Behavioral level descriptions or Functional RTL), and functional graphical representations) as contrasted to structural (architecturally dependent) components (e.g., structural schematics, structural flowcharts, structural netlists, structural RTL, and Boolean Equations). The invention uses the architecture independent functional representations and "generates therefrom the detailed information needed for directly producing an application specific integrated circuit (ASIC) to carry out those specific functions."[10]

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2. **[VISUAL]** The patented process, "for the first time, opens the possibility for the design and production of ASICs by designers, engineers and technicians who may not possess the specialized expert knowledge of a highly skilled VLSI design engineer."[11]

B. Process:

1. Describing Actions and Conditions-

a. **[VISUAL]** A designer prepares a description (known as a "specification") of the function or behavior of the ASIC (or portion) that is to be produced. The input description "can be defined in a suitable manner" or format.[12]

b. **[VISUAL]** A graphical example of the functional input description is a flowchart. (*See* '432 patent, FIG. 5, which illustrates a sequence of functional operations to be performed by an ASIC). The patent also states that the same specification can be provided in a textual format,

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such as in a list form that provides a listing of statements describing the desired functions to be performed by the ASIC. ('432 Patent at 2:21-34)

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c. **[VISUAL]** In accordance with the patented process, the designer need not be familiar with the hardware components or other structure that is to be included in the ASIC. Thus, the input description or specification does not have to specify the structure or architectural components that are to be included in the ASIC to be produced. The input specification is thus referred to as "architecture independent."

d. **[VISUAL]** The description of architecture independent functions are made up of the operations or "actions" to be performed by (or within) the ASIC and the "conditions" under which such actions are to be performed. The architecture independent specifications do not specify or imply the specific structure to be designed.

2. Storing in a Knowledge Base-

a. **[VISUAL]** The patented process uses a storehouse or database of knowledge (known as a "knowledge base") to serve as a base for reference in designing an ASIC. In particular, in accordance with the '432 patent, the knowledge held by experts in VLSI design is obtained and stored in the knowledge base.[13] The expert knowledge is stored in the knowledge base using "rules."[14]

b. **[VISUAL]** "Rules" are prescribed guides or accepted procedures. In the context of the '432 patent, the rules are used to apply the expert knowledge captured from VLSI designers to automatically design an ASIC. The "rules" can take any of a variety of formats. In the preferred embodiment, for example, the rules can be represented using an "IF-THEN" (e.g., antecedent-consequent) format.[15] Other formats are possible, such as pattern-match or other antecedent-consequent format.

3. Storing a Set of Definitions-

a. **[VISUAL]** The functional input specification is translated or "mapped" to an intermediate form to facilitate use by any system used to perform the process. In particular, the desired functions (in the form of "architecture independent actions

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and conditions") are associated with (or "mapped") to a set of definitions of the architecture independent actions and conditions.[16]

b. **[VISUAL]** In the '432 patent specification, an exemplary embodiment uses definitions in the form of code words ("referred to as "macros") representative of a desired function.[17]

c. **[VISUAL]** The set of definitions are typically stored in a library. In the exemplary embodiment disclosed in the '432 patent, the definitions are stored as "macros" in a "macro library."[18] Examples of "macros" can be seen from Table 1 of the '432 patent.[19]

4. Storing Hardware Cells-

a. **[VISUAL]** The hardware components to be used in the design of the ASIC to be produced are referred to as "hardware cells." The hardware cells are basic circuit components (e.g., logic gates, transistors, etc.) that have been previously designed by VLSI engineers, having various functional and technical specifications.[20] A set of available hardware cells that can be used in the design of the ASIC is stored in a "hardware cell library."[21]

5. Operation of the Patented Process

a. **[VISUAL]** The process starts with a user describing a series of architecture independent functional actions and conditions to be performed by the ASIC to be produced.

b. **[VISUAL]** Definitions are then specified from the library of definitions for the desired actions and conditions as described by the user.

c. **[VISUAL]** Hardware cells capable of performing the desired actions and conditions are selected from the hardware cell library by applying the expert knowledge encoded in the rules stored in the expert system knowledge base.

d. **[VISUAL]** A listing of the hardware cells as selected are listed, together with a listing of the connections between such cells, in what is known as a "netlist." FIG. 2 shows an embodiment that generates a netlist using a flowchart input.

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e. **[VISUAL]** The netlist is transformed into a layout of hardware cells that is used to produce the mask data that is directly used for the production of the desired ASIC. The '432 patent shows that other CAD tools (e.g., existing VLSI layout and routing tools) may be used to generate mask data from a netlist. (*See* '432 patent at FIG. 2, and at 4:44-46).

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f. **[VISUAL]** The process also involves the generation of signal lines carrying data signals (known as "data paths").[22] This generation of "data paths" can be performed, like the selection of hardware cells, through the application of expert rules stored in a knowledge base to the selected cells.[23]

g. **[VISUAL]** The process further involves the generation of control signals (known as "control paths") between the hardware cells.[24]

h. **[VISUAL]** Performing the inventive process effectively replaces the need for an expert circuit designer who was, before the invention, required to apply the designer's expertise to the design process to create structural and layout representations of the design.

i. **[VISUAL]** Without the burden of designing the specific structure and layout, even the design engineers who do not have the specialized knowledge of VLSI design could successfully design ASICs faster and more accurately.

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[1] '432 Patent at 1:13-17.
[2] '432 Patent at 1:13-17.
[3] '432 Patent at 1:19-26.
[4] '432 Patent at 1:19-26; and 3:59-65.
[5] '432 Patent at 1:45-51.
[6] '432 Patent at 1:63-66.
[7] '432 Patent at 1:66 to 2:1.
[8] '432 Patent at 1:66 to 2:1.
[9] '432 Patent at 1:38-44.
[10] '432 Patent at 2:6-14.
[11] '432 Patent at 2:14-20.
[12] '432 Patent at 2:21-24.

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[13] '432 Patent at 5:6-8.
[14] '432 Patent at 8:65 to 9:5.
[15] '432 Patent at 11:1-14.
[16] '432 Patent at 9:8-18; and 13:2-31.
[17] '432 Patent at 5:20-22.
[18] '432 Patent at 5:20-22.
[19] '432 Patent at 5:20-22.
[20] '432 Patent at 5:15-20.
[21] '432 Patent at 4:68 to 5:3.
[22] '432 Patent at 2:39-40; and 6:28-54.
[23] '432 Patent at 4:63 to 5:13; and 13:55-56.
[24] '432 Patent at 2:36-44; and 4:63 to 5:13.